Research on the Effective Detection Methods of Large Scale IC Fault Signals

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Abstract. With the continuous development of electronic technology and the unceasing improvement of manufacturing process, large scale integrated circuits (ICs in abbreviation and IC for its single form henceforth) has now become more and more complex. In modern high-tech industrial equipment, however, its core component is one or a few key large scale ICs. So fault detection for these circuits directly determines qualified rate of the product as well as affects the normal operation of the electronic equipment at the later stage. Therefore, the research on effective fault detection methods for large scale ICs has very important practical meaning.

Introduction

The development of large scale ICs has been growing faster and faster while the application fields are also expanding. They have now led to rapid rise in the integration level of ICs; the increase of the scale and density of ICs have directly made their digital relationship more and more complex. This has also caused a lot of difficulties for their production, maintenance and test process. Especially now IC tests occupy a very large proportion in the total cost, so the expensive test cost have rendered imminent research on fast and efficient detection methods. In addition, relevant test theories and practice of integrated circuits technology, which lag behind the circuit scale expanding speed have constitute the main contradiction in large scale integrated circuit detection. This paper, from the perspective of the theories related to ICs, explores effective fault signal detection methods for ICs.

Detection Methods for Large Scale ICs

According to their functional structure, ICs can be divided into analog, digital and mixed-signal types. Among them analog ones are used to generate, amplify and process all kinds of analog signal, wherein input and output signals are characterized by certain proportion relationship between each other. Digital ICs are applied in a wider range than digital ones as they are employed in the current large mechanical and electronic equipment to generate, amplify and process all kinds of digital signals. Digital ICs are characteristic of a certain logical relationship presented by the output and input signals at any time.

IC fault detection is divided into two aspects: fault detection and fault location. As IC design is more and more intelligent, IC fault detection technology has evolved from the early manual detecting and the method of exhaustion into today's digital model, fault dictionary, fault tree analysis, and even to the expert diagnosis system of ICs, detection method based on BP neural network and other intelligent detection methods. Moreover, measuring objects have also gradually evolved from voltage into current.

An Explanation of the Detection Methods for Digital ICs

Large scale ICs are often referred to as those with logic gates between 100-9999 and on a single chip that has been integrated more than 1000 electronic components. The so-called IC fault detection is

developed in terms of the defects of logic function of the circuit, so judging whether there exist faults in a component is by means of judging whether the logic functions of the component can be performed at the request of its design. Logic errors can certainly found out by exhaustion detecting in combinational circuits, but the test efficiency is too low. After repeated research and analyses, IC faults can be successfully dealt with by means of constant fault model to determine corresponding relation between the defects and faults, namely, by assuming the logic fault of the external port fixed for "1" or "0". The practice has proved that this detection method can detect most of the faults. The following is about the specific detection methods.

Fault Detection of Combinational Circuits. The output state of a combinational circuit, at any time, only depends on the input state at the same time, having nothing to do with the previous state of the circuit. A combinational circuit contains the common AND-OR-INVERTER, or their combination. When the amount of input ports exceeds four, the method of exhaustion will be very complicated to employ due to extreme increase of numerical value of the image. It is revealed through the study that when the number of single stage gates at the input port is n, the detection can be completed within n+1 test. Hence we call it the n+1 method. The specific steps of the manipulation are as below: Firstly, assume a combinational circuit with n inputs and m output, then every input n signals have corresponding m ones. Secondly, we can use a vector to represent input and output signals (X_1, X_2...X_n, Y_1, Y_2, Y_n) and defined it as the I/O vector. By transferring the vector into the form of a matrix, then we get the matrix constituted by the input signal of the vector that is called a test matrix. Thirdly, for a gate that has n inputs and one output, if there are logical symbols and a matrix as shown in Fig. 1, this gate can be judged as trouble-free. It can be known from the matrix of n+1 line that it is impossible for any "0" to occur in the AND gate and form the previous n vectors that there is no possibility for any single "1" fault to occur. To sum up, the existence of any single fault is the precondition of that of any multiple faults in a single stage combinational circuit. The cause is that multiple failure test ignores some failures and only highlights the single fault condition. The test vector of the single fault is the above-mentioned vector. If there is no longer a single fault then m corresponding out-gate circuits will necessarily non-existent for multiple fails. Hence, the fault detection is reduced to 2 (m+n) tests.

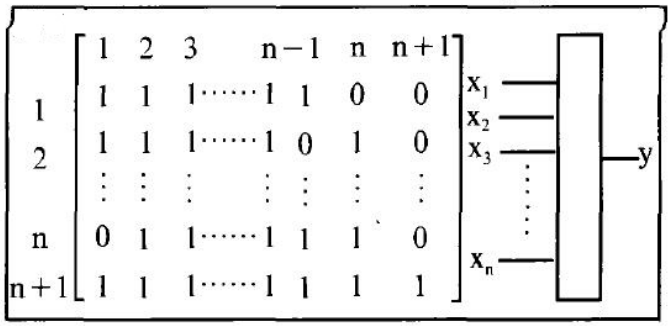

Figure 1 Matrix model as trouble-free

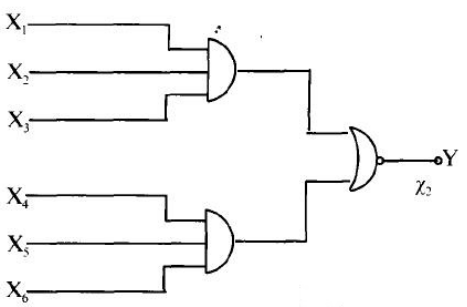

Figure 2 Logical notation for and-or-inverter circuits

A common combination of circuits with AND-OR-INVERTER is often confronted in detecting 74LS51, its logic symbols as shown in figure 2. The logical expression is very simple. The input signals are 6 and the test should be done at least 64 times. And because the two AND gates are symmetrical, the process will be more simplified. Through the analysis, we have found that it can complete the test very well as shown in Fig. 3.

$$\begin{pmatrix} 0 & 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 \end{pmatrix}$$

Figure 3 Test output

We can know from the test matrix that for a two stage combinational circuit the single fault test, after writing the input matrix for each gate, can reassemble the primary gate to generate and simplify the test matrix of the secondary gate. Thus, it has simplified the I/O matrix to a great extent. Then from the theory of logic circuit analysis and verification, the supplement of certain I/O vectors for auxiliary matrix analysis and verification makes the fault test method able to be used in any single fault I/O matrix. The detection method can also be attempted in terms of multistage gate process. The advantages of this approach are that the logic in the process of the validation is very clear and less error-prone and that it greatly simplifies the test times. The only shortcoming is that it needs to go through theoretical analysis and demonstration and that the process of supplementing vectors requires a lot of calculation.

Combinational logic circuit is an important part in IC. In the previous section, we use the single fault assumption, but for the combination of the multistage gate circuit, the approach of single fault assumption and verification is not able to complete the test process very well. The cause is that multiple faults affect the sensitization pathway of single fault assumption, thus making the measuring process failed. But through the single fault detection process can be derived a lot of faults. Therefore, it is adopted in terms of fault detection of large scale ICs.

Detection of Sequential Logic Circuit. A characteristic of sequential logic circuit is that each output state is not only related to the input state, but also dependent on the original state of the circuit. According to the functional difference common sequential logic circuits are ranged among counters, trigger, latches, etc. This section, starting from the test of several typical sequential logic circuits, will explore the detection methods for the sequential logic circuits in large scale ICs. 74LS373 is a kind of 8D latches, its logical function as shown in Fig. 4. Figs 5 and 6 are the corresponding test sequence diagram and show the basically completed state of all the tests. For the test of basic JK flip-flop the method shown in Fig. 7 can be used, which can complete all the tests for J, K, Q as well keep the input signals all the same for the CLK when detecting CLK↓at the same time. This avoids the existence of competitive adventure phenomenon. In the actual process of sequential circuits detecting, detailed sequence of synchronization partition and booting should be inferred according to the flow scheme of the circuit under test. On this basis, the detecting sequence should be inferred so as to complete the detecting process of the whole circuit. Due to the effect of the synchronous sequence of JK flip-flop can be achieved through a simple step of setting 0 or 1, and during the process there is only one output

quantity Q taken as the detecting object, so it can be fully displayed in the partition sequence. Here, the detection process of sequential logic circuit proves to be completely correct.

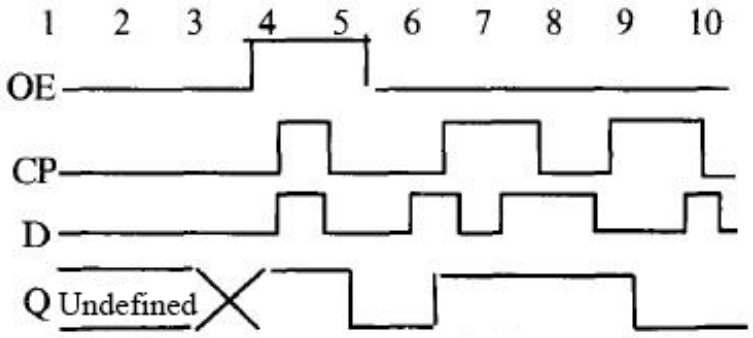

Figure 4 Diagram of Function Sequence

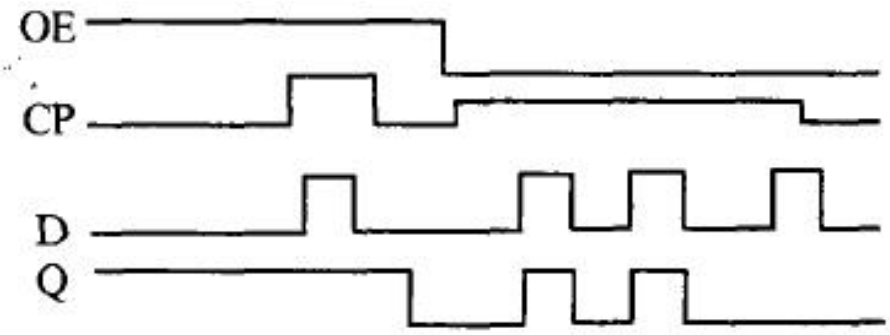

Figure 5 Detection Sequence Diagram with Q Preset as 0

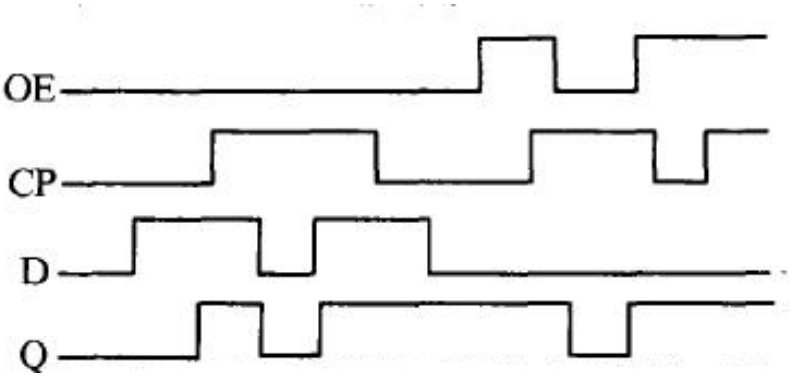

Figure 6 JK Detection Sequence Diagram

Summary

There are many approaches to detect large scale IC, e.g. detection method based on current, neural network pathway, fault generating, etc. However, these detection methods, whether in fault detection or localization process, are all for the basic logic components in ICs including. This paper, multum in parvo, has introduced effective methods for detecting faults in large scale ICs through a simple detection of combinational logic circuits and sequential circuits.

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