An 1.2GHz High-performance MUX-DDFS Using Quartet ROMs

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***Abstract*—This paper presents a detailed description of a direct digital frequency synthesizer(DDFS) using optimized quartet ROMs. The quartet ROMs technology allows improving the system's working frequency with respect to controllable chip size and beneficial effects on system performances. Such a high-speed DDFS has been fabricated and characterized in 0.13 μ m CMOS technology and it produces a 12-bit outputs with a spectral purity of 53 dBc. Its maximum operating frequency is 1.2GHz by using six pipelining stages. Analytical investigation of spectral performances achievable by using dual-slope approximation and detailed description of high-speed flip-flops employed in 1.2GHz DDFS are also presented in this paper.**

***Index Terms*—DDFS, current steering D/A converter, MUX-DDFS, mixed signals integrated circuits**

Ⅰ INTRODUCTION

Direct Digital frequency synthesizers (DDFSs) are able to generate single-phase or quadrature sinusoids with frequency resolution in the sub-hertz range, good spectral purity, very fast frequency switching and phase continuity on switching[1]. Owing to their unique characteristics, DDFS plays an important role in modern communication systems (including spread spectrum and frequency hopping systems), in measurement instrumentation, in radar and in electronic warfare systems. The basic DDFS architecture was firstly introduced by Tierneyetal in 1971[2]. Fig. 1 shows a simplified schematic of a DDFS. The phase accumulator is an overflowing f-bits accumulator that produces a digital sweep with a slope imposed by the value FCW of the frequency control word. The most significant bits are input of the sine/cosine generator, which computes sine and cosine functions with high speed and accuracy. Analog outputs, when required, are generated by digital to analog converters. The frequency of output sine wave signals is proportional to the frequency control word (FCW) which is the clock frequency.

$$F_{out} = \frac{FCW}{2^f} f_{clk}, \quad 0 \le FCW \le 2^{f-1} \tag{1}$$

Where f_{clk} is clock frequency.

The parameter which properly characterizes the DDFS spectral purity is the spurious-free dynamic range (SFDR), defined as the ratio of the amplitude of the desired frequency component to that of the largest undesired frequency component. The most critical block in a DDFS is the sine/cosine generator, which limits operating frequency and is the main source of power dissipation. A number of techniques for phase to sine/cosine amplitude conversion have been published [3]–[5]. These techniques can be subdivided in three categories:

1) look-up table-based approaches[3];
2) angle-rotation algorithms[4];

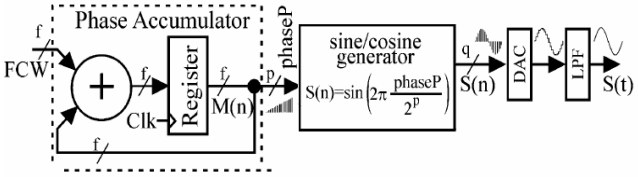

Figure 1. schematic of a quadrature DDFS.

3) polynomial interpolation techniques[5].

The paper is organized as follows. Section 2 describes the DDFS architecture. Section 3 explains the design considerations. In the section 4 and 5, measurement result and conclusions will be drawn.

Ⅱ DDFS ARCHITECTURE

Fig.2 shows the structure of a DDFS system based on the Quartet ROMs. On one hand, wide phase accumulators are often used in DDFS for the fine frequency resolution at high clock frequency, but it cannot finish one addition in a short single clock period because of the delay caused by the carry bits propagating through the adder, to improve the working frequency, a pipeline structure is implemented in it; on the other hand, to overcome the technology constraints to obtain 12-bit linearity, a modified segmented DAC architecture and a new switching scheme, called Q2 Random Walk strategy, were developed, The goal of this work is to obtain good harmonic performance even at high frequencies. System-level analysis led the customer to request 12-bit resolution. Secondary specification parameters were the chip die area and total power consumption. contains all the linear, binary, and input biasing current sources. The converter current is scalable, and up to 5mA can be sourced into external 100-Ω resistors, giving a 1V differential swing at the output.

As we know, the sine/cosine generator section has a most complexity in the system, its limitation of working frequency should be the size of the Quarter ROMs, system-level analysis led the customer to request 10-bit resolution and excellent INL and DNL. Secondary specification parameters were the chip die area and total power consumption.

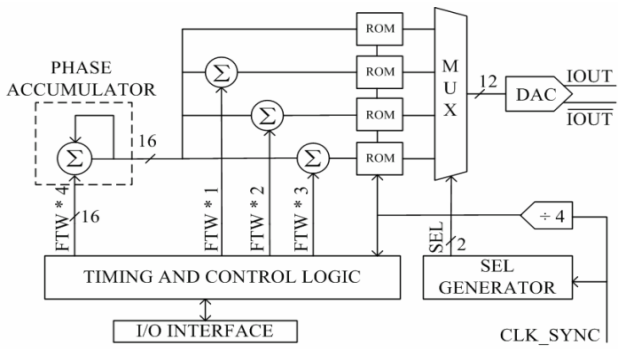

Figure 2. DDFS system with Quartet ROMs

A wide-bits phase accumulator is often used in DDFS for the fine frequency resolution at high clock frequency, and the wide-bits accumulator cannot finish one adding operation in a short single clock period because of the delay caused by the carry bits propagating through the adder. Every new frequency input word is moved into the pipeline circuit. The circuit consists of D-flip-flops (DFFs) and delay elements. The speed of the accumulator based on this architecture can be increased up to m times, where m is the number of stages of the accumulator pipelined. The accumulator in this work is set as 4 stages of 8 bits each, as shown in Fig. 3. Compared with Yuan Ling's method of implementing a segmented nonlinear DAC, it may improve the working frequency distinctly.

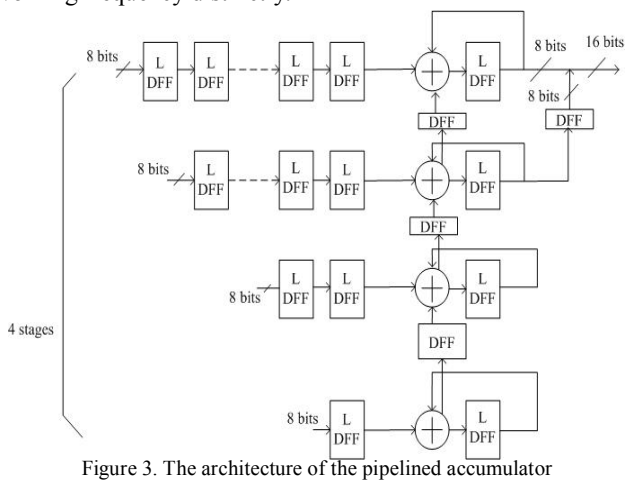

Figure 3. The architecture of the pipelined accumulator

III QUARTET ROMS SCHEME

As we know, the sin/cosine generator section has a most complexity in the system, its limitation of working frequency should be the ROMs, If we can solve the problem of synchronization, Quartet ROMs would be some an excellent method to improve the working frequency. Therefore the traditional look up table is divided into 4 memory sections and a selector. The 4:1 integrated MUX of the MUX-DDFS offers the users the capability to apply an input data rate 4 times lower than the effective sampling frequency used:

$$Data\_rate = f_{CLK\_SYNC} / 4 = f_{CLK} \quad (2)$$

Where f_{CLK} is the frequency of Data Ready clock, since this input MUX is not programmable, all 4 ports have to be used for proper operation of the DAC. Fig.4 shows the internal structure of the sine block. In order to ensure the validity of the digital system, a group of integrated ROMs are set into it. A first step toward the reduction of sine/cosine generator complexity consists in truncating the least significant bits (LSBs) from the phase accumulator. This introduces spurious noise in the DDFS outputs, which should be carefully taken into account in the design phase. Another common approach almost always used to simplify the sine/cosine generator exploits the quadrant symmetry of trigonometric functions and trigonometric identities.

For a MUX-DDFS, this reduces the task of the sine/cosine generator to the calculation of sine and cosine functions for angles belonging to the interval only. For single-phase DDFS, sine calculation for phase angles belonging to the first quadrant is required. To reduce the ROM $\pi/2$ size, the Sunderland technique based on simple trigonometric identities is used in this work. although this introduces the 1/2 least significant bit (LSB) offsets into the output sequence, significant savings in ROM size can be achieved. The phase of a quarter of a sine wave is decomposed to and are, respectively, the MSBs, the middle bits, and the LSBs. The sine function can be expressed as follows:

$$\sin(\alpha+\beta+\gamma) = \sin(\alpha+\beta)\cos(\gamma) + \cos(\alpha+\beta)\sin(\gamma) + \cos(\alpha)\sin(\gamma) \quad (3)$$

The most significant two phase bits are used to decode the quadrant, while the remaining 14 bits are used for the one-quadrant phase to sin amplitude converter. The remaining 14 phase bits are divided into three bit slices: α, β, and γ, having 4, 6, and 4 bits, respectively. Now equation (3) can be rewritten as follows:

$$A_{mpc} = \sin(\alpha+\beta) = \sum si(\alpha)ci(\beta) \quad (4)$$

$$A_{mpc} = \cos\alpha \sin\gamma \approx \sum si(\alpha)fi(\gamma) \quad (5)$$

α is used to generate signals $si(\alpha)$ to control two blocks: Input Latch and MUX. The block of Input Latch is used as power gating block to hold or pass the data of β, γ and 2MSBs to one of eight phase to amplitude generator logic blocks. In every clock cycle, β, γ, and 2MSBs are used as inputs of one phase to amplitude converter logic block only, and the inputs of other phase to amplitude converter logic blocks are unchanged and no dynamic power is consumed. To improve the SFDR performance, 2MSBs are introduced to the one-quadrant phase to sine amplitude converter to reduce the error resulting from 1's complement approximation, which is used to determine whether the sine amplitude is increasing or decreasing. With such structure, we have limited the scale of high speed circuits as much as possible.

Ⅳ Implementation

The chip is implemented in a 1-poly, 8-metal 130nm CMOS technology, and occupies an active area of 0.33 mm ×0.66 mm(core area). The micro-photo of the chip is shown in Fig.5. It includes 3 blocks including digital circuit, BANDGAP and DAC blocks. The DAC core is placed in a separate array to avoid coupling from the digital signals to the current sources. A clock driver is used between the input differential clock pads. The system clock is amplified by the clock driver in the chip. With modern EDA tools, the clock-tree is carefully built to ensure an acceptable clock skew, the maximal delay of the metal wire in chip is about 50ps.

Ⅴ Measurement Result

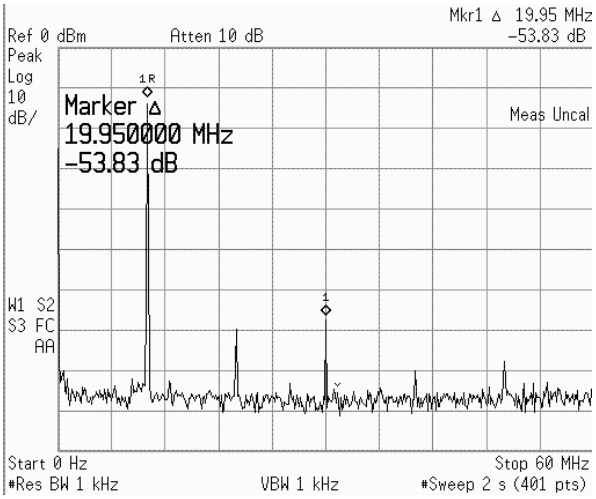

Figure 4. Output spectrum $f_{out}=19.95MHz@1.2GHz$

The DDFS has been fabricated in a 0.13-μm CMOS process and occupies the die area of 0.33mm ×0.66mm, the rolloff of total area is 0.218mm2. It was measured at a single power supply of 1.2V and the maximum output current for a pair of 100Ω termination resister is 5mA to obtain the maximum single-ended analog output voltage of 0.5V. Fig.3 shows the measured spectrum at 19.95MHz output frequency, while the input clock frequency is 1.2GHz. Fig.4 shows the dynamic testing result of the synthesizer. Timing and power dissipation performances have been obtained by simulations with the inclusion of parasitics. The maximum operating frequency is 1.2GHz at room temperature and 1.4GHz at 0 ℃.

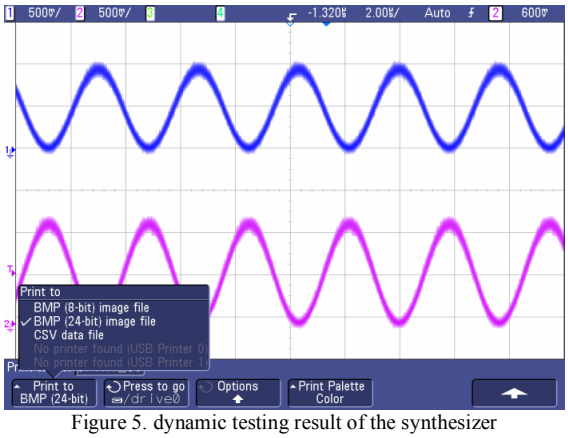

Figure 5. dynamic testing result of the synthesizer

Ⅵ Conclusion

The paper presents the design of a 1.2V 12-bit 1.2GHz CMOS MUX-Direct Digital Frequency Synthesizer. In order to improve the working frequency and spectral purity of the synthesizer, an original quartet ROMs structure was brought forward. Its wideband and narrowband SFDR is about 53dBc and 68dBc while the operating frequency is 1.2GHz.. The synthesizer implemented in TSMC 0.13μm CMOS technology was fabricated. The chip die area was 0.218 mm2, and the total power consumption was less than 74mW with 1.2V power supply.

References

[1] A.Van den Bosch, M.Borremans, M.steyaert, and W.sansen, “A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter,” IEEE J. Solid-State Circuits, vol.36, pp. 315-323, Mar.2001

[2] J. Bastos, A.Marques, M.Steyaert, and W.Sasen, “A 12-bit intrinsic accuracy high-speed CMOS DAC,” IEEE J.Solid-State Circuits, vol.33, pp. 1959-1968, Dec.1998

[3] G.Van Der Plas, J.Vandenbussche, W.Sansen, M.Steyaert, and G.Gielen, “A 14-bit intrinsic accuracy Q2 Random Walk CMOS DAC,” IEEE J. Solid-State Circuits, vol.34, pp. 1708-1717, Dec. 1999

[4] J. Hyde, T.Humes, C.Diorio, M.Thomas, and M.Figueroa, “A 300-MS/s 14-bit digital-to-analog converter in CMOS,” IEEE J. Solid-State Circuits, vol.38, pp.734-740, May.2003

[5] A.Van den Bosch, M.Borremans, M.Steyaert, and W.Sansen, “A 12b 500 Msample/s current-steering CMOS D/A converter,” in IEEE Int. Solid-State Circuits Dig. Tech. Papers, Feb.2001, pp.366-367