The Design and Implementation of FFT Algorithm Based on The Xilinx FPGA IP Core

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Abstract—**This paper introduces a kind of FFT algorithm design and realization based on the Xilinx IP core . On the analysis of FFT algorithm, Rely on Xilinx Spartan -3A DSP FPGA series as platform, by calling FFT IP core, validating the feasibility and reliability in FFT algorithm medium or lower end FPGA.**

Keywords-FFT algorithm module, Xilinx IP core, Spartan -3A DSP, Fixed-point compression

I. INTRODUCTION

FFT (Fast Fourier Transform) algorithm is the high efficient algorithm of calculating DFT. Originally algorithm is proposed by J.W.Cooley and J.W.Tukey in 1965, and later new algorithms constantly emerging, in a word development direction have two: one is for N = 2 integer times power algorithm, such as base 2 algorithm, and base 4 algorithm and split base algorithm, etc; Another is N is not equal to 2 integer times the algorithm, such as meal factor algorithm, Wino grad algorithm etc. One base 2 algorithm is currently common FFT algorithm, its core thought is to decompose of the sequence of N points into (N - 1) / 2 points, finally decomposed into 2 points DF T and calculated, thereby eliminating DFT large numbers of repeated computation of DFT. FFT algorithm can decompose of sequence from time domain or frequency domain: (1) decimation in time (DIT) namely directly divided the sequence x (n) on the odd and even to the odd and even son sequence , then through calculating the son sequence DFT to realize the whole sequence DFT; (2) decimation in frequency (DIF), and divided the number of frequency x(k) on the odd and even to the even and odd points son sequence, then calculate son sequence of DFT, get the DFT of whole frequency domain. The calculation complexity and need the amount of calculation of decimation in time and frequency are the same, and by two different methods decomposition form: DIT need to rearrange to input data sequence x(n), frequency extraction method requires to rearrange to output data sequences x(k). Currently FFT algorithm has been used widely in digital signal processing, image processing, oil exploration and earthquake prediction etc. Meanwhile, in order to facilitate FFT algorithm application in engineering practice, each big FPGA producers also have put forwarded related function of IP (Intellectual Property) module base. Among them the IP core Fast Fourier Transform V5.0 Xilinx produced by Xilinx company offered multiple-selectable calculation parameters, structure, data input/output flow order way of FFT algorithm, can easily realize FFT algorithm according to the needs of the users.

II. XILINX FFT IP CORE FUNCTIONS

Xilinx IP core function is hardware description language (HDL) design documents based on complex system function , these validation function for all the Xilinx FPGA device structure can reach optimization, and provide hardware description language (VHDL Verilog) function simulation model, can be in the design and debugged in standard EDA simulation tools .

Xilinx FFT IP core V5.0 put forwarded by Xilinx company mating the FPGA development tools ISE10.1, its biggest system clock frequency reached 550MHz, the maximum data throughput reached 550MSPS, highest can undertake 65536 point FFT operations, maximum input data and phase factor wide for 24bit (bitwidth larger, the dynamic range greater, support all the mainstream) Xilinx FPGA chip. Meanwhile, Xilinx FFT IP core V5.0 can be realized transformation length is N point of real or plural form of transformation FFT and inverter FFT change (IFFT), N scope is (8 ~ 65536). Input data real part plural part should be showed with bitwidth M bits of Two-Complement form, M value range is (8 ~ 24); Similarly, phase factor bitwidth scope is also (8 ~ 24). Data, phase factor and output data double-ranked cache data in FFT realization process, can use Block RAM or Distributed RAM to storage. For I/O architecture Burst, block RAM can store any points of data and phase factor, while distributed RAM can only store points no greater than 1024 point data and phase factors; For Streaming I/O structure, can be use mixed storage method, Firstly choose to use the order number of block RAM memory, then adopt the distributed RAM for remains.

Xilinx FFT IP nuclear has four kinds of structure can be choosed, the user can choose between the number of logical resources using and the length of convert time ,concrete cases as follows.

(1) assembly line, Streaming I/O structure: allows continuous data processing, use the most logical resources;

(2) base 4, Burst the I/O structure: provide data import/export stage and processing stage, import data and processing the data separately. This structure has smaller structure, but the conversion is time longer;

(3) base 2, Burst the I/O structure: use less logical resources, went with four stages, provide two stage process.

(4) base 2 Lite Burst the I/O structure: this is a kind of based on base 2 structure variants, adopted the time multiple method with a minimum of logic resources, but the conversion time is longest.

For Burst the I/O structure, use DIT method; Line, Streaming I/O use DIF method.

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In the actual hardware operation, the module execution speed is very important parameters, this paper is based on the assembly line, the simulation validation of Streaming I/O structure do the continuous data processing. Line, Streaming I/O architecture adopt assembly line technology design to a series of base 2 wing processing engine, and each wing processing engine has its own independent memory to input data and intermediate data (figure 1). In this structure, FFT IP nuclear has also deal with the current frame N point data, load the next frame N point data, output an ancient frame N point before data ability.

Xilinx FFT IP nuclear V5.0 support three algorithm types: full precision no compression, block floating-point and fixed-point compression (compression ratio by user-defined).

For all the precision no compression structure, any a meaningful integer in data channels will be retained, the decimal part produced during the operation will be truncated or integer. This structure, for fixed-point algorithm, after multistage multiplication operation later, data bits wide will double its output bitwidth, increasing input for (input bitwidth+log2 (data conversion length) + 1) bits.

For Block floating-point type, any data point in one frame data have the same compression ratio, the compression ratio as the output value by Block Exponent shows, and only in FFT IP nuclear testing will produce a data, we will do compression operations.

This paper adopted the fix-point compression structure. This structure, compared to full precision no compression structure can greatly reduce the FPGA internal resources Xtreme DSP Slices and the use of block RAM, and relative to block floating-point type, can be adjusted flexibly compression ratio. The compression ratio chart(Scale_SCH) of fixed-point compression structure. Compression ratio is according to 1, 2, 4, or 8 for each order compression, namely separately shift right corresponds to 0, 1, 2 or 3. If compression are inadequate, the output wing will become beyond the dynamic range, cause data overflow. For Burst I/O architecture, Scale_SCH's expression methods: for each stage compression ratio are made by appointed 2bits number, the zero stage 2bits number are the lowest 2bits zero order, concrete for [... N4 , N3, N2, N1, N0], each 2bits number respectively correspond to the corresponding stage compression ratio. For example: to base 4 structure, data transfer length N = 1024, Scale_SCH = [01 10 00 11 01]for stage 0 right shift bit 2, stage 1 right shift bit 3, stage 2 right shift bit 0, stage 3 right shift bit 2, stage 4 right shift bit 1. Experience conclusion (can prevent to produce data overflow) : for the base 4 structure 1024 point, Burst I/O architecture, Scale_SCH = [10 10 10 10 11]; But for the base 2 structure 1,024 point Scale_SCH = [01, 01 01 01 01 01 01 01 01 10].

For assembly line, Streaming I/O structure, put near a pair of base near 2 bands group together, namely stage 0 and stage 1 for group 0, stage 2 and stage 3 is group 1, etc. Scale_SCH expression methods: for each group of compression ratio are made by appointed 2bits number, the 2bits number of zero group is the lowest, concrete form for [... N4, N3, N2, N1, N0], each 2bits number respectively correspond to the corresponding group of compression, said the two base 2 of same group have the same compression ratio. Example: the data length N = 1024, Scale_SCH = [10 10 00 01 11] for group 0 (stage 0 and stage 1) right shift bit 3, group 1 (stage 2 and stage 3) right shift bit 1, group 2 (stage 4 and stage 5) no shift, group 3 (stage 6 and stage 7) right shift bit 2, group 4 (stage 8 and stage 9) right shift bit 2. If transform lenth N is not 4 integer times power, the last group only contains a base 2 bands, can use 00 or 01 said. Experience conclusion (can prevent to produce data overflow) : N = 512, Scale_SCH = [11] 01 10 10 10; N = 1024, Scale_SCH = [10 10 10 10 11].

Compression ratio, the Scale_SCH bitwidth for assembly line, Streaming I/O architecture and base 4, Burst the I/O structure, for 2 * ceil (0.5 * log2 (N); For base 2, Burst the I/O structure and base 2 Lite Burst the I/O structure for 2 * log2 (N), including N for converting data length.

III. FFT IP CORE OF SIMULATION VALIDATION

Through invoke Xilinx IP core to achieve a 512 points, data bitwidth. and phase factor for 16bit bitwidth of FFT algorithm modules, clock frequency for 50MHz (clock frequency higher, can obtain higher reuse multiples, save more resources area), uses assembly line, Streaming I/O and fixed-point compression structure, complete in the commissioning medium or ower end FPGA, verify its reliability and feasibility. In order to facilitatly verify the correctness of the nuclear function of FFT IP core: with zero start counting, in every clock rise along comes, add an operation obtained data respectively as real part and plural part of input signal. Scale_SCH = [01 10 10 01 11], in ISE10.1 build engineering, in invoke Xilinx FFT IP core, then use SE6.5 ModelSim to simulate, the simulation timing as figure2shows.

Timing validation aspects: the whole timing sequence is entirely correct. As can be seen from the timing diagram: signal high indicates that FFT IP core is ongoing FFT operations, after doing signal down that operation to have ended, the output FFT operation result; Edone signal done signal in a cycle reached before; At this time, a cycle, done market-place complete; that FFT operations And, because of the 512 points, so, each operation FFT 512 clock cycle, interval edone and done signal will push a; RFD signal has been pulled that input data has been transferred to FFT IP core of input ports, Streaming with using line, I/O architecture continuous data processing, are consistent; Dv signal is high, show for the output signal is effective.

A functional verification aspects: according to FFT IP core in assembly line, in Streaming I/O architecture, interval each frame data need three frames can output the characteristic of the calculation results, can calculate inside the simulation above output corresponding to the [94: moments [94:605] + [94:605]* j FFT output results. Inside the Matlab simulation result, according to the proportion of Scale_SCH compress, and it is consistent with the result shows that the FFT IP core woeking is normal .

IV. CONCLUSION

This paper mainly through FFT IP nuclear overall testing and validatiing FFT algorithm the feasibility and reliability

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in medium or lower end FPGA. In selecting lines structure realize FFT basis, adopts fixed point, reduce the time of data reading and processing, better meet the needs of the FFT processing data.

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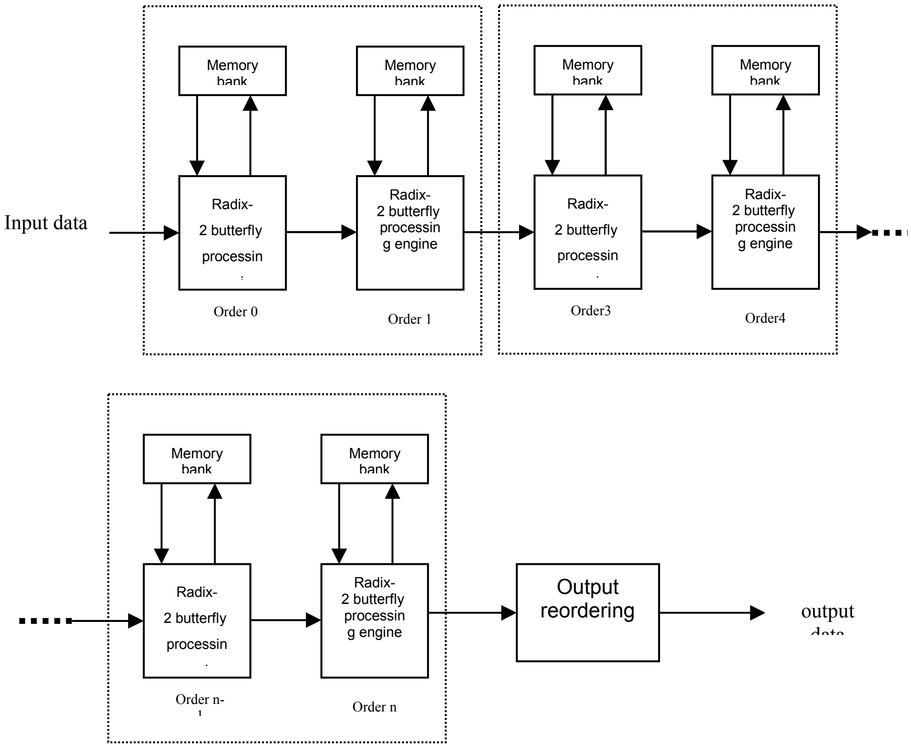

Figure 1. FFT module assembly line, Streaming I/O structure

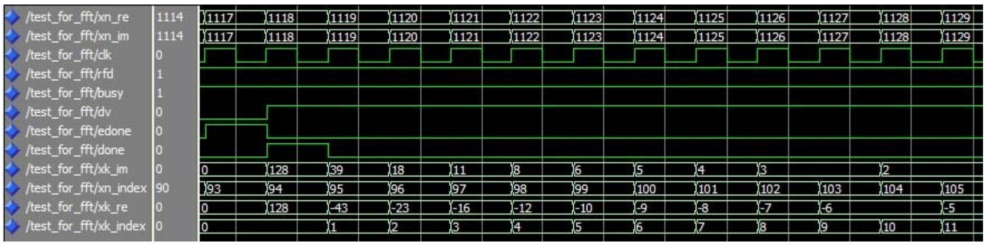

Figure 2. FFT simulation results local figure