

# Design of Lfmcw Radar Level Measurement System Based on Sopc

Liang Ling

College of Electrical Engineering and Automation  
Jiangxi University of Science & Technology  
Ganzhou 341000, China

Lai Fengqin

College of Mechanical and Electronic Engineering  
Jiangxi University of Science & Technology  
Ganzhou 341000, China

**Abstract**—Aiming at the special conditions that it is very difficult to measure precisely and continuously by the traditional level measurement. This paper designed the linear frequency modulation continuous wave radar level measurement system base on SOPC. The paper introduced the overall design of the system, and elaborated on the function of hardware and software implementation of SOPC system . T

**Keywords**-Level measurement, SOPC, Linear Frequency Modulated Continuous Wave Rada

## I. INTRODUCTION

In the smelting and chemical production processes we often encounter in a large number of solid and liquid materials. Level is a very important process parameter. Through the accurate measurement of the material level, the operator can take response measures on the production based on changes of material level. In the complex modern technology production process, especially in the dicky measurement conditions such as the mixing tank, high temperature, large steam, corrosive medium, easy scarring, and the operator is far away from the scene, the real-time accurate measurement of the material level is particularly important for the optimal control and the safety of the production process. It can become the key to automatic production of the enterprises[1].

Linear frequency modulation continuous wave (LFMW) radar measures the distance through modulating the continuous wave emitted and using the frequency and the phase of the echo information. It is a more advanced level measurement method because of the prominent advantages such as high accuracy, free from environmental restrictions. The current study just emerged in the field of level measurement at home and abroad, it will has a broad application prospects[2].

## II. OVERALL SYSTEM DESIGN

The radar level measurement system includes two parts: data acquisition and SOPC system . Data acquisition is using the antenna of radar to transmit and receive the echoe of the material level. It exports mixing frequency signal through the integrate front part of radar. After pretreating it forms digital signal through A / D converter. And it controls the linearity of VCO by using the correction of the sawtooth wave voltage signal exported through the A / D converter.

SOPC system includes 3 parts: FPGA, memory, and the external interface. FPGA is built on the FPGA chip, and the core is the Nios processor . The design uses the chip

EP1C12Q240C8 of series Cyclone. In FPGA, the A / D and D / A conversion and control modules are achieved by writing VHDL program; DSP module is designed by DSP Builder in Matlab; the remaining parts are designed in the SOPC Builder[3].

According to the functions and the determined programs of system, the overall structure of system is shown in figure 1:

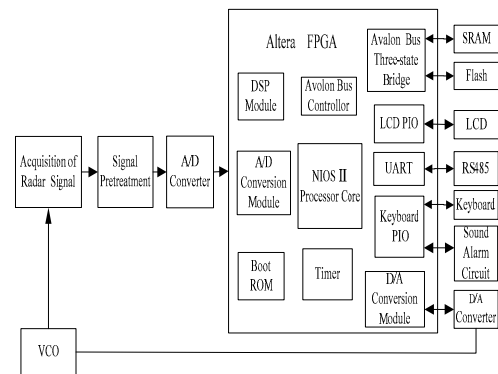


Figure 1. The overall structure of system

## III. HARDWARE DESIGN BASED ON SOPC SYSTEM

### A. Design for the Signal Acquisition Circuit

The signal acquisition circuit of the linear frequency modulation continuous wave radar is composed by radar transmitter and receiver, preamp , matched filter, automatic gain amplifier, A / D converter and Nios soft core processor and other components[4]. And its block diagram is shown in Figure 2.

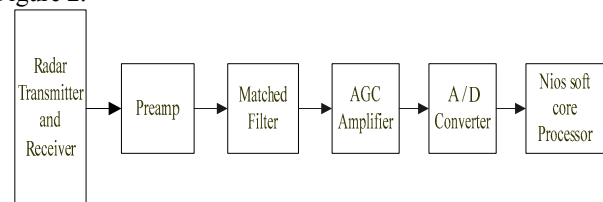


Figure 2. Diagram of the radar IF signal acquisition circuit

### B. FPGA function implementation of the embedded soft core NIOS

The hardware design of Nios II processor is based on the system functional requirements. It customs appropriate CPU

and peripherals, then it is implemented in SOPC and Quartus II.

According to the system's requirements, Nios II processor should be configured the following components and interface module: cpu、onchip\_ROM—system boot、uart1—system simulation debugging、uart\_rs485—RS485 communication interface、Timer1—system internal clock、ext\_ram—external SRAM、ext\_flash—External flash and the A / D, D / A conversion interface module、key\_pio—matrix keyboard interface、lcd\_pio—LCD interface and some PIO ports, the module is shown in Figure 3[5][6].

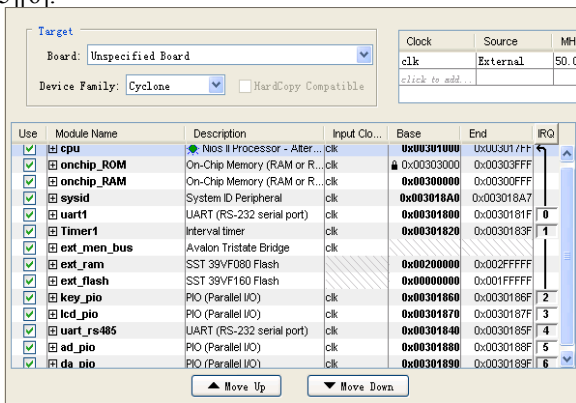


Figure 3. NIOS II module map

Designed in this setting based on SOPC, the generated Nios system module is shown in Figure 4:

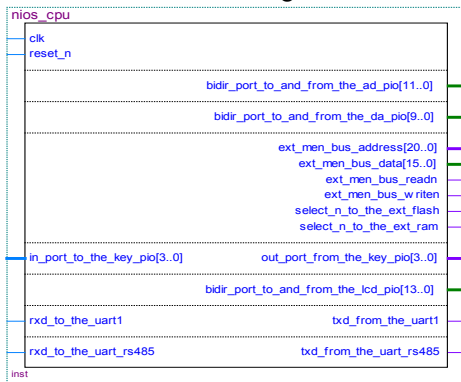


Figure 4. System module diagram based on Nios

### C. Design and Implementation of the Data Acquisition and Control Module

In SOPC Builder it provides some peripheral interface modules, but the A / D conversion interface module is not ready-made, we need to write VHDL program to customize the peripherals. The A / D conversion for the radar IF signal is using the A / D converter AD9226. It is a differential input 12-bit A / D converter. The VHDL code of AD9226 control module is written as follows:

```
LIBRARY IEEE;
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USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
ENTITY ad9226 IS
PORT(Data_of_ad : IN STD_LOGIC_VECTOR(11
DOWNT0 0);
CLK_state : IN STD_LOGIC;
START : IN STD_LOGIC;
CLK : OUT STD_LOGIC;
Q : OUT STD_LOGIC_VECTOR(11
DOWNT0 0));
END ad9226;
ARCHITECTURE behav OF ad9226 IS
TYPE states IS (st0, st1, st2, st3,st4,st5,st6,st7,st8) ;
SIGNAL current_state, next_state: states :=st0 ;
BEGIN
CLK <= CLK_state;
P1: PROCESS(current_state)
BEGIN
IF(START='1') THEN
CASE current_state is
WHEN st0=>Q <=Data_of_ad;
next_state <= st1;
WHEN st1=>Q <=Data_of_ad;
next_state <= st2;
WHEN st2=>Q <=Data_of_ad;
next_state <= st3;
WHEN st3=>Q <=Data_of_ad;
next_state<=st4;
WHEN st4=>Q <=Data_of_ad;
next_state <= st5;
WHEN st5=>Q <=Data_of_ad;
next_state <= st6;
WHEN st6=>Q <=Data_of_ad;
next_state <= st7;
WHEN st7=>Q <=Data_of_ad;
next_state <= st8;
WHEN st8=>Q <=Data_of_ad;
next_state <= st0;
WHEN OTHERS=>next_state <= st0;
END CASE;
END IF;
END PROCESS P1;
P2: PROCESS (CLK_state)
BEGIN
IF (CLK_state'EVENT AND CLK_state='0' )
THEN
current_state<=next_state;
END IF;
END PROCESS P2;
END behav;
This program generates the A / D conversion and control module AD9226 and the circuit symbols is shown in Figure 5:
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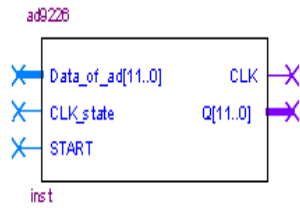


Figure 5. AD9226 Control Module

The simulation result of the control module AD9226 is shown in Figure 6:

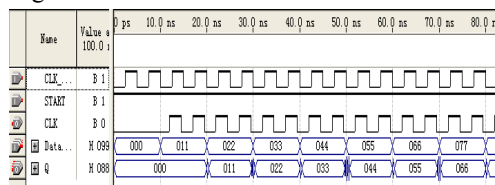


Figure 6. Simulation timing diagram of the control module ADC9226\_CTL

#### D. Hardware Design of the Input and Output Modules and Communication Modules

The input and output devices and communication modules of system are composed of the matrix keyboard, LCD screen, sound alarm circuit and industrial control network interface.

The input device is a  $4 \times 4$  matrix keypad, it is customized peripherals of the Nios II CPU through the method of a 4-bit input and output PIO port accessing to Avalon bus. To meet part of the level measurement work in outdoors and prevent lightning and static electricity damaging to the communication system, the communication interface RS485 uses the chip SN65LBC184 produced by company TI. In SOPC the Nios is configured a UART and connects with the external circuit composed of chip SN65LBC184. The sound alarm circuit adopts 555 multivibrator circuit model, and connects with the key PIO. LCD uses the liquid crystal display GDM12864A, it is connected with the PIO port configured by the Nios.

The programs of system will complete the following functions. Such as the control of data acquisition, FFT power spectrum estimation, RS485 communication, LCD liquid crystal display and matrix keyboard. According to the design and the work process of the system, the flow chart of the main program is shown in Figure 7.

#### IV. SOFTWARE DESIGN OF SYSTEM

The programs of system will complete the following functions. Such as the control of data acquisition, FFT power spectrum estimation, RS485 communication, LCD liquid crystal display and matrix keyboard. According to the design and the work process of the system, the flow chart of the main program is shown in Figure 7.

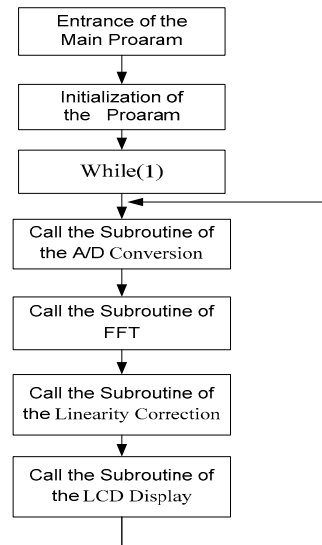


Figure 7. The flow chart of main program

#### V. RESULTS AND METHODS OF DEBUGGING

The node signal datas of system can be observed in real-time by using the embedded logic analyzer SignalTap II in the Quartus II. The signal observed can be displayed by the any numerical or the waveform. The results show that the LFMW radar level measurement system based on SOPC has greatly improved on accuracy and processing speed than the conventional measurement device. And it is conducive to the optimal control of the production. Therefore, The level measurement system in the industry will have broad prospects.

#### REFERENCES

- [1] HE Xiao-dong, ZHENG Hua. Different Materials Level Measurement Method [J]. Road Machinery & Construction Mechanization, 2002, (5): 22 ~ 24
- [2] YANG Quan-li, XIE Ke-ming, YAN Gao-wei. Modeling and Simulation of an FMCW Radar for Measuring Coal Level [J]. Journal of Taiyuan University of Technology, 2006, (5): 16 ~ 19
- [3] PAN Song, HUANG Ji-ye. SOPC Technology Practical Guide [M]. Beijing: Tsinghua University Press, 2005, 3
- [4] WEI Pei-min. Application of Range Radar in Material Level Measuring [J]. New Technology & New Process, 2002, (1): 8
- [5] LIU De-liang, WANG Zu-lin, WEI Guang-jun. FPGA-based High-precision Frequency Measuring Instrument [J]. Industrial Technology in Hebei, 2010, 27(1): 29-31.
- [6] Li Hua, WANG Yong-li. NIOS System and the Computer Serial Port Communication [J]. Southwest University for Nationalities, 2008, 43(4): 864-867.