A System Design for DSP + FPGA Based Cache-structured Image Processing

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***Abstract*—This essay presents the DSP + FPGA structure based high-performance image processing system. It aims at solving the overtime-processing problem brought by the increasing complexity of images through the cache-structured image-processing driver. This system allows frame-dropping whenever the processing of images runs overtime and achieves one frame. The system simulation result shows in this way the diver achieves higher efficiency than traditional ping-pong mode when dealing with the overtime-processing of images.**

Keywords-Image processing driver, overtime, cache structure

I. INTRODUCTION

With the development of microelectronic technology, high frequency and multi-system signal-processing platform has become the direction where digital signal processing development goes. As the DSP + FPGA structure has a high-speed signal acquisition and processing system for both the easy access to complex algorithm of DSP and good extendibility of FPGA, making itself a popular hardware structure for real-time infrared image processing system.

In the FPGA + DSP image processing system, though the underlying signal preprocessing algorithms such as median filtering and morphological processing require a large amount of computation, but the algorithm is fixed, and the structure is simple, without an impact from the complexity of input image, thus suitable for the FPGA hardware. Though the High-level processing algorithms require less computational algorithms than the lower layer, but it has a more complex structure control, is suitable for the use of DSP chip as well. Although the DSP processor can optimize real-time algorithm through various means, but the limit of itself (the interface bandwidth, less on-chip multiplier than those based on FPGA, smaller memory capacity than PC104) makes the requirement of resources and computational time of some image processing algorithms such as gray threshold segmentation, connected component labeling and track correlation under a bigger impact of the complexity of input images in the DSP-based core-processing image detection tracking system. It makes the processing time of single frame image differ according to its complexity, and even leads to over-time processing of a single frame in the cloudy or sea-sky background. However, in the tracking and detection system, the platform angle measuring and image processing require strict synchronization. A frame drop will result in loss of target information which impacts the tracking stability of detection system. This essay discusses the over-time problem while dealing with the time difference from the perspective of image processing. This approach of replacing the traditional ping-pong buffer with the cache-structured image processing driver achieves good results in practice.

II. SYSTEM HARDWARE STRUCTURE

This design of the infrared tracking of DSP + FPGA based image processing system is shown in diagram 1. The images are input in an analog signal mode and the frame rate is 50Hz. The size of the analog image is converted into 480 * 280 through the AD9246 digital-to-analogue conversion. FPGA adopts EP2C70 of the CYCLONE II series developed by Altera Corporation. The system logic element (LE) is 68,416 and the total memory of configuration is1M bit. The C64XX of TI, with the highest main frequency which amounts to1GHz, has the following integrated peripherals: EDMA controller, the external memory interface (EMIF), multi-channel buffered serial port (MCBSP), hardware platform interface (HPI), General purpose input output (GPIO), interrupt controller, 32-bit timers etc. C64 series is mainly represented by DM642 which has the dedicated video chip and C6416 which has the general processing chip. This essay chooses C6416 as the image processing core not only because of its much higher frequency than that of DM64X (DM64X amounts to 720MHz, C6416 amounts to 1GHz), but also C6416 has two more characters compared to DM64X

1) TMS320C6416 chip has 1M Byte large-capacity on-chip RAM. As the DSP has a multi-level cache structure which makes the processing speed of data differ greatly in different storages, the idea of using on-chip RAM to store the image data will improve the actual image processing speed. In this case, infrared image size is 480 * 390 * 2B = 374.4KB, higher than the 256KB on-chip RAM of DM64x series. The C6416 makes use of the two-dimensional transmission mode of EDMA and puts to be read data from the external cache into the on-chip RAM. It avoids the need for frequent operation of the external data port and at the same time, highly improved the efficiency of image processing algorithms.

2) TMS320C6416 has two interfaces, the 64bit EMIFA and the 16bit EMIFB respectively. TMS320C6416 has two interfaces, the 64bit EMIFA and the 16bit EMIFB respectively. According to the need of image acquisition and cache processing in this article, the data is 374.4 * 3 =

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1123.2KB. It is bigger than the FPGA and DSP on-chip RAM, so there is a need to design cache for the external memory. The two EMIF interfaces of TMS320C6416 bring combination of high-bandwidth and EDMA, which can make the image acquisition, transmission and management more efficiently.

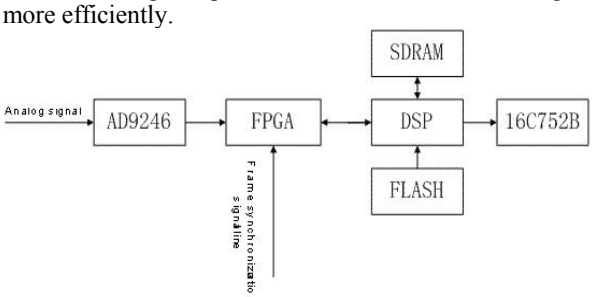

Figure 1. Diagram of Image Processing System

The second diagram shows the connection of main hardware in the image- processing system. In the DSP + FPGA image-processing systems, DSP and FPGA data interface typically use SRAM to build ping-pong buffer. The DSP would put the corresponding image data from SRAM into the on-chip RAM for processing.

Because the bandwidth of external data interface has been widened by two EMIF buses of C6416, the data of FPGA FIFO can be read in rows by EMIFB. First to build interface of the frame buffer in SDRAM of EMIFA sent through the EDMA, then register the full frame data from SDRAM while dealing with it.

Compared to the one reading operation of traditional ping-pong frame buffer, this scheme conducts two reading operations and one writing operation to frame buffer. Though it increases the complexity, but then there is no need to design the frame buffer of SRAM as it reads data in rows through the FPGA interface. The test result shows that in this way it simples the system hardware design and meets the requirements of image data acquisition and transmission bandwidth at the same time.

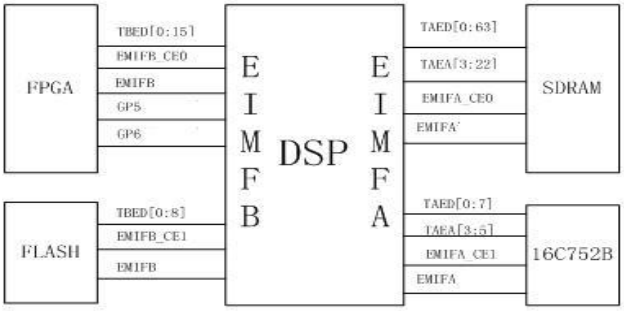

Figure 2. Main hardware connections of the infrared image processing system.

III. DSP-DRIVEN DESIGN OF THE THREE CACHE

Frame frequency of the input image signal system shows the single-frame processing time is 20ms. When it works at night or in the daytime when it's not cloudy, the single frame image processing time is less than 10ms; But when the system works in cloudy days or in the more complex sea and sky background, the gray-scale wide distribution and complex background will lead to segmentation algorithms and clutter suppression algorithm that adds to the complexity, and result in large fluctuations in the frame processing time (Shown in the following diagram) and over-time processing, which influences the stability of the tracking system. In order to solve this problem, we optimized the cache structure of the image processing.

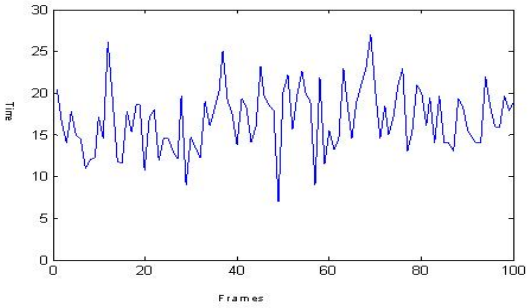

Figure 3. The processing time under complex background

Traditional ping-pong buffer structure consists of the collection and processing of a frame buffer frame that deal with image acquisition and processing alternately, they would change into the other as they finish a pair for each collection and processing of the frame buffer. Obviously in the ping-pong buffer structure, the image processing time is less than image acquisition time. When there occurs the over-time problem in image processing, it will leads to the conflict between cache acquisition and image-processing cache. After fully took the benefits of the ping-pong buffer structure, this essay uses processing cache of three image, processing of frame pointer, the pointer cache to be collected, and a new frame signal in order to design a driver for the three- cache structured DSP.

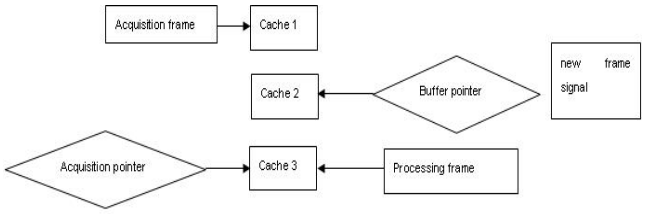

Figure 4. Schematic diagram of the three cache

In the above schematic diagram for the three cache, the three separate cache can do either acquisition or image-processing, and it depends on the pointer of the cache-collecting and the pointer of cache-processing. When the current cache-collect and cache-to-be-collected buffer form a pair put in the ping-pang buffer, the left cache acts as image-processing frame buffer. And the logic of dealing with the change of three cache, the frame pointer, and the pointer of to be collected cache are as follows:

1) When the image acquisition is completed, the update processing frame pointer would point to the current address where stores the cache acquired, read the cache of

the pointer, and collect the other cache in the ping-pong buffer. Then the new frame signal is effective as the pointer points to the newly acquired cache from to-be-cached position.

2) When the image processing is complete, it would read the new frame signal. If the signal is valid, it will deal with deal with newly-acquired frame which the pointer points to. At the same time, it will update to-be-cached pointer into processing frame pointer, and create invalid new frame signal.

When the system processing is not running out of time, the image processing time is less than the frame acquisition time, after dealing with each image. There is a need to wait for a new frame signal, to get the latest address for the acquisition of frame buffer.

When the overtime processing problem occurs in the system, in addition to collecting and processing the frame buffer, the system designs another cache to be collected. When the acquisition is completed, but the current frame processing is not, the system can use the to-be-acquired frame to acquire image data and avoid the conflict between the acquisition and processing of ping-pong buffer. When the current overtime processing frame is finished, it can process the data of the new frame by checking the new frame signal and reading it. So the frame drop of the system is actually a kind of cumulative one, if the cumulative time of processing is more than frame acquisition time, the system dropped frames when it collects two frames in the processing time of one frame. By this time the information of frame drop in this system could be acquired through the new frame signal detection system. When the acquisition is completed, and when the new frame signal is still valid, the system would drop one frame, the target information can be obtained through the extrapolation of the former two frame target information.

Main module procedures are as follows:

```
While(1)
// main processor
                {
                        While(New frame) ;
//check for new frame of image
                        Ima buf exchange(0);
          // update the image cache
                        New frame=0;
            //update frame processing mark
                        EDMA_set Channel (img_buf);
// EDMA reads the frame data processing
                        DELAY(delay time);
           //wait for the finish of DELAY
                        Img process();
                  // image processing
                }

                Interrupt GP5()
                // line interrupt program
                {
                        EDMA_setChannel(img_line);
//EDMA reads a new line of data
                        Line_counter++;
                // line counter counts
                        Line_addr=linecounter+480*2;
          //line address counts
                        EDMA_reconfig();
//re-configure the EDMA destination address parameter

                }

                Interrupt GP6()
                //the frame buffer interrupt process
                {
                Img buf_exchange (1);
                        //update the image buffer
                If(New frame);
                        //identify frame drop
                Target predict ();
                        //Target predict
                New frame=1;
                          //update image process mark
```

IV. RESULTS AND CONCLUSIONS

In the test, it aims at testing the occasionally overtime and continuous image processing respectively. In the former test, the system continuously collected 10,000 frames and deal with 9901 of them. In handling the image frame, there are 673 frames whose processing-image time runs over 20ms. But due to the three-cached structure, though these frames take up the processing time of the next frame, they did not result in the loss of the next frame. There are 99 frame-drops due to the accumulation of continuous time out. In the test of continuous time-out, the image processing is replaced with a delay of 25ms process.

In the procedure as there were delayed collection of EMDA and the storage time, it turned out that the acquisition and processing time is 25.21ms for each image. The system acquired 10,000 frames continuously, and it actually dealt with 4981 frames using the traditional ping-pong buffer. With the three-cached design, the number of actual processing amounted to 7933, which reached the goal of the designed.

This paper introduces a FPGA + DSP based image processing system, and the use of the three cache to design DSP image driven approach. The practical results show that when the system works in complex background for example in cloudy days, there were fewer frame drops caused by over-time process than that with the traditional ping-pong mode. In the accumulated frame-dropping cases, extrapolating target information helps reduce influence on the tracking stability of the tracking system and achieves good results.

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