A Sequential Circuits Test Set Generation Method Based on Ant Colony Particle Swarmalgorithm

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Abstract—**There exists a lot of trigger unit in Timing circuit, and this leads to high computational complexity in its initialization and test set generation for deterministic method. This paper presents a timing circuit initialization and test set generation method. In the proposed method, a particle swarm algorithm is used to initialize the sequential circuits, and correlation matrix of the circuit is transformed into a graph, and finally ant colony algorithm is used to generate the corresponding test set. In the contrast experiments, it is demonstrated that the generated test set is able to complete the initialization and fault detection for the ISCAS' 89 benchmark timing circuit, and the coverage rate of production meets the actual demand, and the iteration times and execution time shows obvious advantages.**

Keywords—Test set generation, Ant colony algorithm, Particle swarm algorithm,Timing circuit

I. INTRODUCTION

With the development of the LSI, it takes great challenges for the test of the timing circuit. And the difficulty mainly lies in the following aspects: Firstly, there exists a great mount of trigger and memory in the timing circuit, and they should be initialized in the testing process; Secondly, the timing circuit tests code length is much greater than the combined circuit, it is a series of test vector set representing different functions, including the initialization, fault activation, and its propagation.

The deterministic sequential circuit testing method has high computational complexity, therefore, people are more inclined to study the test method based on simulation, in which the most widely used method is genetic algorithms GA. Corno[1] points out by contrast that that GA based test set generation algorithm is better than the senior logic and symbolic test generation algorithm. Then, Bhuvaneswari improved the crossover, mutation and the fitness model, and increased the the fault coverage rate [2]. But, the GA algorithm still has the premature phenomenon, Li Zhi et al. proposed a ant colony algorithm based sequential circuits testing generation method [3], this method contains circuit initialization and test vector generation. This paper made further discuss by combining particle swarm optimization and ant colony algorithm for the initialization of sequential circuits and test sets generation.

II. SEQUENTIAL CIRCUIT INITIALIZATION

A. the existing research on Sequential circuits test generation

In the timing circuit , the initial state of each storage element is unknown , so how to set up triggers' initial state is a difficult problem. For the sequential circuit existing the general line in circuit design, it is feasible of reseting all the units. But for the circuit there is no clear line, you need to find a match test series to guide the circuit to a determined state. Somenzi [4] used binary decision diagram method to generate the initialization sequence , but this method requires a lot of memory when describing the circuit, and therefore is applicable for smaller circuit only. Keim [5] combines the binary decision diagram and greedy algorithm to generate the initialization sequence. And Wahbeh [6] introced genetic algorithm to the timing circuit initialization. These two methods shows good effect, but endure the shortcoming of long execution time, and cannot be applied to large scale circuit, Li Zhi [7] applied ant colony algorithm to the timing circuit initialization process successfully. in his method, the trigger is looked as food, and generate the initialization sequence using ant path. But this method only used one individual ants, so can not realize parallel execution, and the execution time increases when the circuit scale increases.

Circuit initialization can be divided into functional and logical initialization. The current automatic test generation tools and commercial fault simulator support logical initialization, so a lot of studies are focused on this method. In this paper, an improved particle swarm optimization algorithm is used in timing circuit initialization phase, and in the subsequent work, the further research is made on sequential circuits test vector generation.

B. The basic model of the sequential circuit

The general sequence circuit and its corresponding combined model are shown in Figure 1, where C (T) is a combinational circuit. And its input signal from the original input X (T) and storage element output of S y (T). The relationship between X (T), Z (T), Y (T), y (T) is as followings:

$$Z(t) = Z(y(t), X(t))$$
$$Y(t) = Y(y(t), X(t))$$
$$y(t+1) = y(Y(t))$$

It can be seen that a duplicate logic array is formed by combining n +1 period models at t = 0,1 , ..., n +1. By this

way, the time division is transformed to the division of space , each separate partition is a combinational circuit , that is a timing circuit is transform into a combinational circuit .
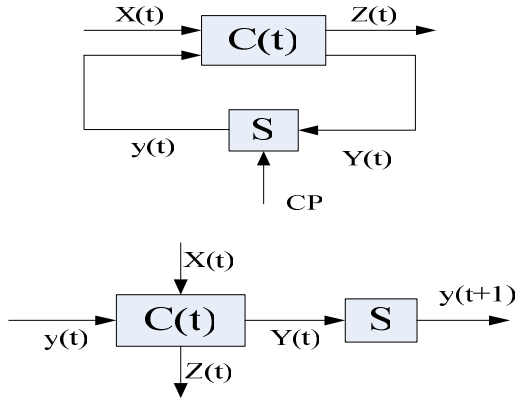

Figure 1 Synchronous sequential circuit structure and the combination model

III.   INITIALIZATION FOR SYNCHRONOUS SEQUENTIAL CIRCUITS AND TEST SET GENERATION

A.   Initialization for synchronous sequential circuits

Timing circuit test sequence is composed of 0,1 string. and the initialization sequence is a special kind of test sequences. usually, initialization vector and the vector in the evolutionary process of the groups are together looked as as the quasi - initialization vector.   When these quasi - initialization vector are jointly applied to the circuit, the initialization result is returned through the fault simulation. And when all triggers are initialized in the circuit or there is no more trigger to be initialized, it is regarded as the end of the initialization process.And at the same time, the initialization sequence and trigger state is output. ,The algorithm processes is shown in figure 2.
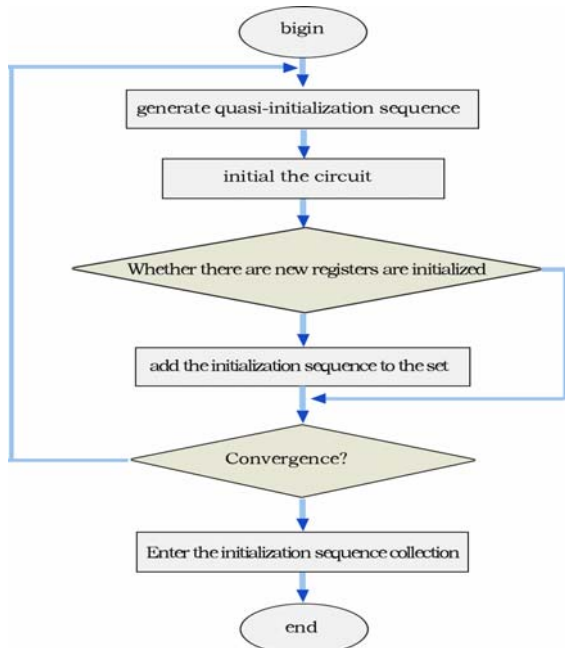

Figure 2 Timing circuit initialization flowchart

0, 1 codes of individual particle are used in representing the original input, and the coding length is consistent with

the circuit original length. and the fitness function is defined by the number of initialized triggers at each time.

$$fitness(i, j) = (1-\alpha)(num(x_{i,j}) - num(gbest_{i-1}))$$

The fitness function   indicates the initialized triggers number for the jth particle individual at the generation ith. On behalf of the i of j particle vector joined to the circuit, all can be initialized number of triggers, corresponding to represent the i-1 of j particle vector can initialize flip-flops number, called the updating coefficient, namely in the i-1 generation has the initial trigger for the initialization of the trigger ratio.

Evolution rules are as follows:

$$w = w_0 - (w_0 - w_f)\Box t / T$$

$$v_{ij}(t+1) = w\Box v_{ij}(t) + c_1 r_1(p_{ij}(t) - x_{ij}(t)) + c_2 r_2(g_{ij}(t) - x_{ij}(t))$$

$$x_{ij}(t+1) = \begin{cases} x_{ij}(t) & v_{ij}(t+1) > v_{ij}(t) \\ x_{ij}(t) & \text{Other} \end{cases}$$

Algorithm for the introduction of rebellious particles , that each iteration of the distance to target the most distant individual position best, and set the gradient coefficient , with the iteration number   is incremented rebellion of attenuation.

The best position of particles and rebellious groups corresponding   relation   can   be   expressed as:
$$x_{ij}(t+1) = \begin{cases} x_{ij}(t) & v_{i\lambda}(t+1) > v_{i\lambda}(t) \\ x_{i\lambda}(t) & \text{Other} \end{cases}$$

B.   Sequential circuit test sets generated

For a known structure of multiple output circuit, its associated matrix can clearly reflect the circuit input and output structure relationship, therefore can be associated with the corresponding matrix into a graph structure, and the use of ant colony intelligent algorithm for further solving.

1)   Correlation matrix conversion

Multiple output circuit is usually divided into two kinds, one is the output of the circuit and all of the original input signal are related, the structure is equivalent to a single output circuit of simple combination, can use a single output circuit block partition method to solve; second is the circuit output with only a portion of the input correlation, so in the test portion of the circuit which only use part of the input, while the remaining unused input for free, for these free items can be used as the other output terminal when the valid input, thus can further reduce the required test number.

With the following relation matrix $D(N)$:

$$D(N) = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

In order to reduce the test vector quantity according to the following principles $D(N)$ for block:

a) Listed as units of matrix partition;

b) After dividing each every line in not only contains a 1 element;

c) Partition number at least.

Can get the following two block:

$$DP(N) = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$ or

$$DP(N) = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

Input variables $J_i = (x_{i1}, x_{i2}, ..., x_{il})$ $i = 1, 2, ..., p$

Which correspond J_i to the two value for:

$$J_{i0} = (x_{i1}, x_{i2}, ..., x_{il}) = (0, 0, ..., 0)$$
$$J_{i1} = (x_{i1}, x_{i2}, ..., x_{il}) = (1, 1, ..., 1)$$

Then the corresponding test vector:

$$J = (J_1 J_2 .... J_p)$$

A total of value , each independent block output only and the blocks in the input, so the combination will be able to complete the exhaustive testing circuit.

2) Test set generation algorithm

For Figure $G(V, E)$, the vertex $V = \{v_1, v_2, ...v_n\}$ sequence representation, the shading color $C = \{c_1, c_2, ...c_n\}$ set representation, and made the following definition:

$D(n \times n)$ said the adjacency $G(V, E)$ matrix, and to meet vi do not reference V

$$D(i, j) = \begin{cases} 0 & \\ 1 & \end{cases} \quad \text{vi is referenced Vj}$$

$S(n \times p)$ for Coloring table , coloring matrix, to meet the: Vi do not bepaint cj

$$S(i, j) = \begin{cases} 0 & \text{Vi is bepainted cj} \\ 1 & 代小组 V_i 有 c_j 凸 \end{cases}$$

$$\sum_{j=1}^{p} S(i, j) = 1$$
and

Ant individual k after $S(i, j)$, select to the node coloring c_j to represent prime matrix v_i , the initial value of the pheromone matrix $\tau(n \times p)$ are constant , corresponding

pheromone $\tau(i, j)$ concentration of node coloring c_j , coloring matrix $S(n \times p)$ with one relationship, $\Delta_k \tau(i, j)$ said the ants k in the node coloring c_j is selected , the legacy of pheromone concentration , the update formula can be expressed as :

$$\tau_{ij}(i, j) = (1 - \rho)\tau_{ij}(i, j) + \Delta\tau(i, j)$$

$$\Delta\tau(i, j) = \sum_{k=1}^{m} \Delta_k(i, j)$$

$$\Delta\tau_k(i, j) = Q / Numc$$

the algorithm flow chart is as follows :
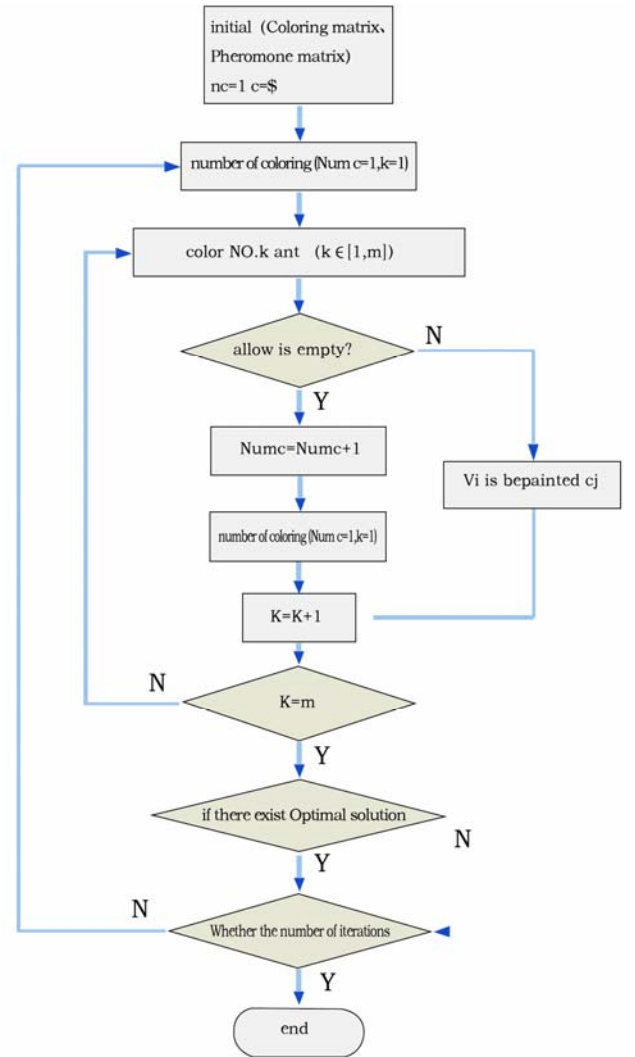

Figure 3. ACTSG algorithm flow chart

IV. EXPERIMENTAL DATA AND CORRELATION

A. Experimental data sets

The ISCAS85 ISCAS89 ISCAS93 is a series of internationally recognized standards circuit , usually as an effective verification platform has been widely used . For the proposed timing circuit initialization and test set generation method , select the ISCAS'89 benchmark sequential circuits

as the experimental data set contains the number of fault can be measured within

B. Timing circuit initialization results contrast

ISCAS'89 benchmark sequential circuits obtained by the PSO algorithm initialization sequence is shown in table 1 :

TABLE I. BASELINE SEQUENTIAL CIRCUIT INITIALIZATION SEQUENCE

Circuit name	State sequence	Circuit name	State sequence
S27	010	S400	111110111111111111111
S208	00000000	S444	00000000000000111100
S298	00000001111100	S526	000000010000001110100
S344	000111111111111	S641	0000111010010011111000
S349	000111111111111	S713	10111011101111110011
S382	001011000000000000000	S820	00000
S386	001100	S832	00000
S1238	111011011000010110	S1488	000000

The timing circuit initialization phase, this paper selects the genetic algorithm ant colony algorithm GA [8], AA [7] as contrast, three kinds of algorithm initialization results as shown in table 2:

TABLE II. INITIALIZATION RESULTS

Circuit name	Failure number	GA			AA			PSO		
		INIT	LEN	CPU(s)	INIT	LEN	CPU(s)	INIT	LEN	CPU(s)
S27	3	3	1	0.2	3	1	0.017	3	1	0.018
S208	8	-	-	-	-	-	-	8	2	0.02
S298	14	14	2	0.8	14	2	0.00	14	2	0.00
S344	15	15	2	1.1	15	2	0.00	15	2	0.00
S349	15	15	2	1.0	15	2	0.00	15	2	0.00
S382	21	21	1	0.8	21	1	0.017	21	1	0.016
S386	6	6	2	1.2	6	2	0.017	6	2	0.015
S1238	18	18	1	3.5	18	1	0.017	18	1	0.017
S400	21	21	1	0.9	-	-	-	21	1	0.02
S444	21	21	1	0.7	21	1	0.017	21	1	0.019
S526	21	21	2	1.2	21	2	0.00	21	2	0.00
S641	19	19	1	1.9	19	1	0.017	19	1	0.016
S713	19	19	1	2.2	19	1	0.033	19	1	0.037
S820	5	5	1	0.1	5	1	0.033	5	1	0.031
S832	5	5	1	0.2	5	1	0.017	5	1	0.016
S1488	6	6	1	2.7	6	1	0.050	6	1	0.048

Through the comparison of the experimental data in Table 2, we can found that the genetic algorithm and particle swarm algorithm shows advantages in the initialization for synchronous sequential circuits. In detail, the execution time is advantageous, similar magnitude, but the genetic algorithm for certain basic circuit can not be given proper initialization vector (S208, S400), in this part of the circuit will only be achieved by initialization function to set the initial value. And the particle swarm algorithm rule has the advantages of short execution time and complete initialization. The Particle swarm optimization algorithm requires less parameters than genetic algorithm, And in each iteration, it only needs to update the position and velocity vector. It can been seen from table* that, the initialization time of particle swarm algorithm can be finished within one second, which can be neglected when is contrasted to the generating the test set time. In constrast to the ant colony algorithm, particle swarm optimization algorithm has better parallelism, so the efficiency is higher.

C. Sequential circuits test generation

For the known sequence circuit, the stable operation state based circuit can be got after the initialization activation. In the further testing set generation experiment, this paper will first transformed the incidence matrix to a graph structure, and then use the ant colony algorithm to solve the graph coloring problem, finally obtain the test vector set.

Comparative test selected SPIRIT [9], ATOM [10], and CRIS based on genetic algorithm [11] algorithm in contrast. The contrasted results are shown in table 3:

TABLE III. RESULTS OF TEST SET GENERATION

Circuit name	Failure number	SPIRIT		ATOM		CRIS		ACTSG	
		Detection of failure number	Execution time	Detection of failure number	Execution time	Detection of failure number	Execution time	Detection of failure number	Execution time
S27	3	3	1.741	3	1.638	3	1.014	3	0.879
S208	8	8	15.078	8	14.370	8	8.507	8	6.504
S298	14	14	28.310	14	29.551	14	14.245	14	11.328
S344	15	14	31.225	14	32.470	15	12.610	15	10.083
S349	15	15	42.561	15	40.289	15	27.359	15	20.760
S382	21	21	78.090	21	81.363	21	38.664	21	27.668
S386	6	6	23.451	6	27.560	6	13.056	6	10.435
S1238	18	18	38.508	18	31.437	18	19.334	18	13.276
S400	21	21	64.307	21	62.550	21	31.580	21	27.870
S444	21	19	81.560	19	83.496	21	35.449	21	26.884
S526	21	21	78.372	20	72.441	21	37.210	21	30.176
S641	19	19	84.073	19	88.904	19	32.546	19	24.701
S713	19	19	90.090	18	91.218	19	40.708	19	31.682
S820	5	5	8.710	5	6.452	5	2.316	5	2.011
S832	5	5	11.268	5	10.773	5	1.768	5	0.945
S1488	6	6	15.332	6	16.007	6	2.338	6	2.174

The experiment data shows, CRIS and ACTSG algorithm has higher efficiency, and their execution time is much lower than the SPIRIT and ATOM algorithms. The transformation from the circuit associated matrix to a graph improves the efficiency for the application of ant colony algorithm. At the same time, the application of the bionic algorithm to the test set generation can effectively cover the failure point, and greatly reduce the testing set generation time. Table 1 shows, the PSO and ACTSG algorithms is able to generate a vector set at the stage of initialization and test set generation for sequential circuit, and its its efficiency is better than the constrasted algorithms.

D Summary and Prospect

Focusing on the prolem of initialization and tes set generation for timing circuit, this paper proposed a improved PSO algorithm and ACTSG algorithm. These methods improved the efficiency of test set generation according to the characteristics of different stage in the test of timing circuit. And we just made a preliminary exploration for the combination of two kinds of bionic algorithms. And the further discuss of their parallel implementation and sequential circuit initialization sequence optimization will be held in our future work.

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