Based on Prospective Dynamic Frequency Scale Power Optimize Method for Multi-Cores Processor's I/O System

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***Abstract*—Power problem has been one of the most restricting development barriers of processor. I/O system power is an import part of the processor's power. The paper aims at I/O dynamic power of multi-cores processor, and put forwards a prospective dynamic frequency scale with clock gating power optimize method. The experimental results show that the method which we put forward can greatly reduce the dynamic power of I/O system.**

Keywords- Multi-Cores Processor; Dynamic Power; Prospective; Dynamic Frequency Scale; Clock Gating

I. INTRODUCTION

The transistor's number of single chip has been more and more with increasing size of chip. And with driving of performance, clock frequency raised continuously. Power density increased following with the power Moore lawyer. Power problem has been more and more severe. High power will increase chip's manufacturing cost, decrease reliability, and limit performance play. Low power design has been one of the most import issues of microprocessor design. Power optimization can be done at process circuit-level, architecture level and software level. With feature size shrinking, process circuit-level methods will be ineffective, and software level methods must support by hardware. But architecture level methods not only can significantly optimize power, but also can balance between power with performance, so has been the most effective direction of the optimization. Power consists of storage cell power and clock power. The total power consumption of clock will be more than 40% with running real applications[1]. Clock mesh power can be optimize by effective clock gating method. Paper[2] researched of the optimization of network of chip by clock gating method. Architecture level optimization methods includes voltage/frequency Scale[4-7], clock gating[8-9] and low power coding techniques[10-11] etc.

II. PROSPECTIVE DYNAMIC FREQUENCY SCALE POWER OPTIMIZE METHOD

A. Motivation

Try to stop idle I/O components' clock, and scale frequency of components which have low requests arriving rate and bandwidth utilization according to I/O components busy or not and I/O requests' information. So the dynamic power of I/O system can be reduced significantly. Figure1 showed the working flow of PDFSCG. Once some components' performance which have been scale frequency could not satisfy applications' demands, these components would enter full speed mode. If there have new requests arrive components which clock stop, the clock must be started again in advance, and can be enter scale frequency mode or full speed mode according to I/O requests pattern. To avoid effect performance, I/O bandwidth demand must be warned in advance, so clock can be restarted or scale frequency immediately.

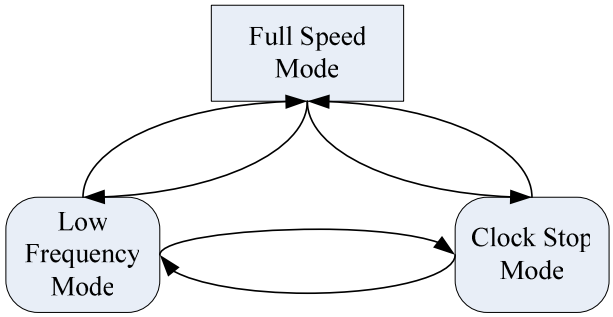

Fig.1 PDFSCG Working Flow

B. Implementation

The control signals generating of clock gating and frequency scale is the key technique of PDFSCG. We adopted fine-grained clock gating, and design independent clock gating logic for each I/O component. Clock gating control signals must be valid immediately, otherwise not only cannot optimize power, but also reduce performance. PDFSCG adopted prospective forecast according I/O data flow to generate clock gating control signals. I/O requests have two directions: from process core and memory flow to I/O(PIO requests and DMA response), and from I/O to process core and memory(DMA requests, interrupt and PIO response). As figure2 showed, we divided I/O system into several sub-modules, and noted as $IODM_{0\sim n}$, $IOUM_{0\sim m}$. UI is upper interface which connects with crossbar and shared cache. DI is down interface which

This paper put forwards a prospective dynamic frequency scale with clock gating power optimize method(PDFSCG) to optimize I/O dynamic power of multi-cores processor.

connects with I/O interface. UI and DI are I/O data entrances of I/O system. UI and DI analyze every I/O request destination, and statistic request arriving rate and bandwidth utilization, and send this information to each I/O sub-module. I/O sub-module would prospective the possibility whether itself would be access to generate the clock gating control signals, and put itself into full speed mode, scale frequency mode or clock stop mode.

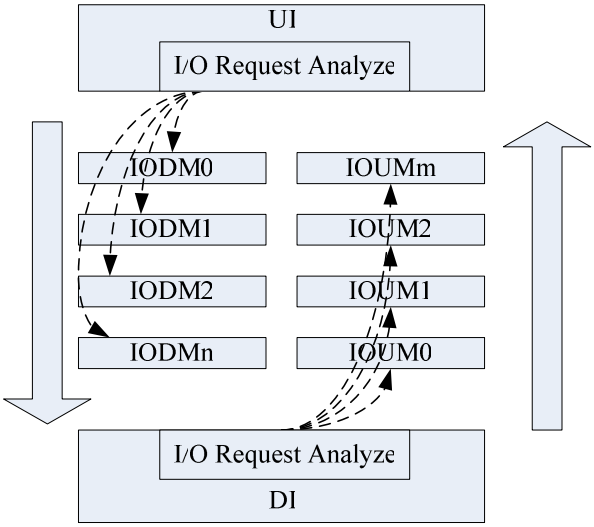

Fig.2 I/O Request Prospective Forecast

Figure3 showed the clock gating logic. Clock select signal Clk_sel selects between different frequency clocks and output I/O clock IO_Clk according to I/O performance request. Clock stop signal controls all input clocks, and stop all output clocks if it is valid, and module enters into clock stop mode. Clock gating logic control I/O sub-module enter which work mode.

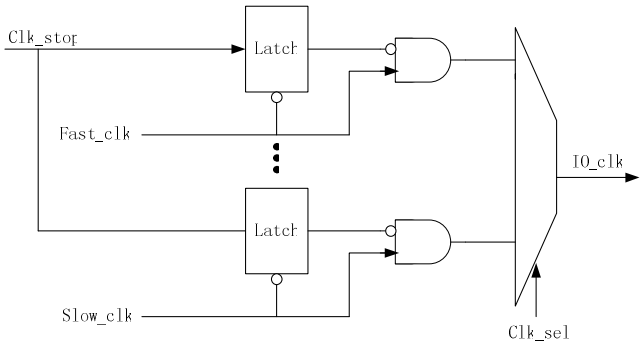

Fig.3 Clock Gating Logic

To reduce I/O dynamic power further, PDFSCG adopted low-weight low power I/O interface coding technique. This method can reduce synchronously switch noise of I/O drivers. PDFSCG added a bit to note whether data need reverse, so can reduce density of continuous 1 and 50% switch noise.

III. EXPERIMENTAL RESULTS

We used Spyglass tool to evaluate PDFSCG power optimization result based on the IOU module of FT multi-core processor chip designed by ourselves. We recorded one week I/O Trace of mail server, FTP server and simulation server. We used these traces as input of IOU simulation environment to get the distribution of I/O clock frequency, and generated VCD files. Spyglass tool analyzed the I/O dynamic power based on these VDC files.

Figure4 is the I/O clock frequency distribution of different trace, I/O full speed clock frequency is 600MHz. We statistic the rate of different I/O clock frequency range, zero showed I/O clock stopped, 100 corresponds to the rate which I/O clock between 0MHz with 100MHz, and so on. As figure4 shown, simulation almost work in full speed mode because always have many test programs running. For FTP server, requests are burst, so always distrusted on high frequency and low frequency. For MAIL server, almost work in low frequency mode because loads are little grained burst.

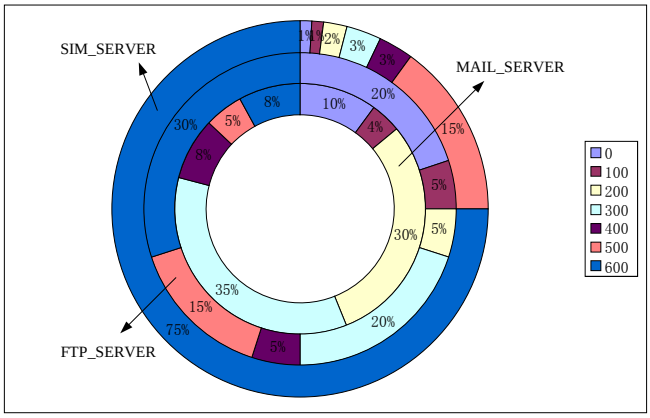

Fig.4 Distribution of Different I/O Trace

Figure5 showed the IOU dynamic power of three I/O applications based on PDFSCG and design without clock gating. As figure5 showed, I/O dynamic power reduced significantly when adopted PDFSCG method. For MAIL server, the power is only half of before, for simulation server, power also reduced 10%.

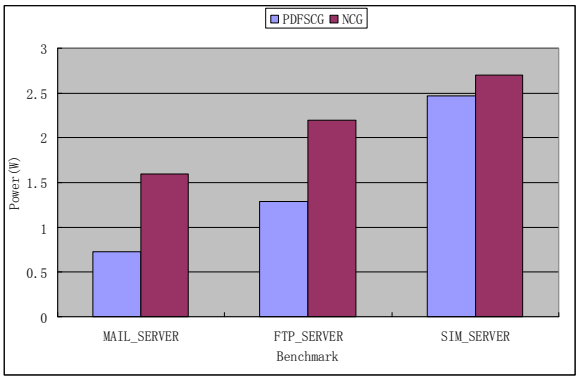

Fig.5 PDFSCG Power Optimization Result

IV. CONCLUSION

With the rapid development of microprocessor, power wall has been one of the most issues which restrict performance improvement. Power optimization techniques have been one of the most key techniques of microprocessor research. The dynamic frequency scale method and clock gating method are very effective methods for power optimization. How to reduce I/O dynamic power without reduce performance is main content of this paper. We adopted prospective dynamic frequency scale power optimize method optimized I/O power significantly, the future work is study on how to realize effective prospective.

REFERENCES

[1] Monica Donno, Alessandro Ivaldi, Luca Benini,Enrico Macii. Clock-tree power optimization based on RTL clock-gating[C]. Proceedings of the 40th Design Automation Conference, Anaheim, CA, United states: Institute of Electrical and Electronics Engineers Inc., 2003: 622~627.

[2] Zhou Hongwei. Research on Memory System and Interconnedt Architecture for Multi-core Processor[D]: National University of Defense Technology, 2010

[3] R. Mai, Z. Y. He, B. Kirby. A novel dynamic frequency estimation algorithm in power system[C]. 43rd International Universities Power Engineering Conference, UPEC 2008, Padova, Italy: Technological Educational Institute, 2008

[4] Jeremie Chabloz, David Ruffieux, Christian Enz. A low-power programmable dynamic frequency divider[C]. 34th European Solid-State Circuits Conference, ESSCIRC 2008, Scotland, United kingdom: Inst. of Elec. and Elec. Eng. Computer Society, 2008: 370~373.

[5] Ying-Chieh Ho, Ya-Ting Chen, Chauchin Su. A power efficient on-chip bus design with dynamic voltage and frequency scaling scheme[J]. International Journal of Electrical Engineering, 2010, 17(Compendex): 207~215.

[6] F. Firouzi, M. E. Salehi, F. Wang, S. M. Fakhraie,S. Safari. Reliability-aware dynamic voltage and frequency scaling[C]. IEEE Annual Symposium on VLSI, ISVLSI 2010, Lixouri, Kefalonia, Greece: IEEE Computer Society, 2010: 304~309.

[7] Hailin Jiang, Malgorzata Marek-Sadowska. Power gating scheduling for power/ground noise reduction[C]. 45th Design Automation Conference, DAC, Anaheim, CA, United states: Institute of Electrical and Electronics Engineers Inc., 2008: 980~985.

[8] Ashoka Sathanur, Luca Benini, Alberto Macii,et al. Multiple power-gating domain (multi-VGND) architecture for improved leakage power reduction[C]. ISLPED'08: 13th ACM/IEEE International Symposium on Low Power Electronics and Design, Bangalore, India: Institute of Electrical and Electronics Engineers Inc., 2008: 51~56.

[9] Dinesh C. Suresh, Banit Agrawal, Jun Yang,Walid Najjar. Energy-efficient encoding techniques for off-chip data buses[J]. Transactions on Embedded Computing Systems, 2009, 8(Compendex).

[10] Dinesh C. Suresh, Banit Agrawal, Jun Yang,Walid A. Najjar. Tunable and energy efficient bus encoding techniques[J]. IEEE Transactions on Computers, 2009, 58(Compendex): 1049~1062.