FPGA Design of Switch Module with Multicast Function on the Satellite Onboard Switch

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***Abstract*—This paper implements a shared memory switching structure with multicast function due to the demand of multicast function on the satellite onboard switch, introduced each module of the ideas and working process in detail. Key modules are programmed and realized with Verilog HDL. The results of ModelSim former simulation show that the circuit satisfies the functions of the shared memory swapping structure, and requirements with low complexity.**

Keywords- satellite onboard switch; shared memory; multicast switch;

I. INTRODUCTION

In recent years, multicast communication has got more and more applications in life. Some typical example such as widespread use of video conferencing, network TV, system notice, distance learning, etc[1]. The satellite communications network is easy to implement multicast switching due to its characteristic of wide coverage, so it has become a trend to achieve the multicast services via satellite. It is a key technology for the satellite onboard switch to successful deal with more and more multicast communication business.

This paper describes the FPGA design ideas and work processes of a satellite onboard switch witch have multicast functions. Multicast communication is what the data packet to input port needs to be exchanged to multiple destination output ports [2]. In Switching fabric, the most commonly and most simple way to process multicast cell is cell replication, and then processing each multicast cell as a unicast cell. However, due to the influence of dramatic changes in ambient temperature and various particles in space, making the available memory type and capacity not like the ground as well-off, the limited internal storage resources of the fabric is not enough to deal with a large number of multicast cells, also the cell replication methods waste input bandwidth [3]. So, in this design, we use the pointer replication way to management multicast cell, in the case of minimizing the storage resources possession, to complete the cell multicast function.

II. STRUCTURAL DESIGN AND WORK PROCESSES OF CELL SWITCHING MODULE

Figure 1 is a basic structure of the shared-memory switching, wherein the cell switching module is composed by main control module, Input interface control module, output interfaces control module, external SRAM and multicast counter.

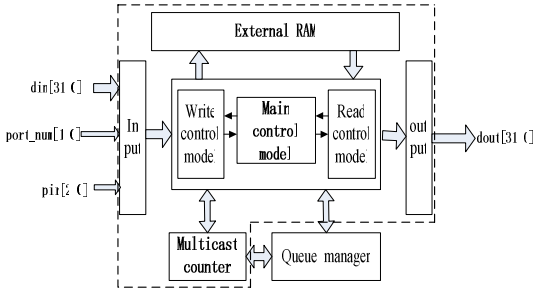

Figure 1. basic structure of shared-memory switching

A. main control module

The mainly responsible for the main control module is to store the input side cell into the external SRAM ,and also the cell which is ready to be read out will be output to the outside of the switching fabric by the main control module.

IP packet in this design is divided into a fixed-length (this design 64bytes) packet (hereinafter collectively referred to as the cell) to be exchanged, external SRAM size is 16K (16384 cells that can be stored), all cell shared external SRAM. The SRAM data 32 bits wide, so that the SRAM every time you can read and write the data of 4 bytes, a cell need to go through 16 write operations can be written into the external SRAM, Similarly, a cell needs 16 times read operations to be read out from the SRAM.

The main control module reading and writing process shown in Figure 2:

a) wait_req: System reset, defined a bit M_RR register to balance the read and write operations between the variable-length packets. when the M_RR is low, first determine the external SRAM whether there write request, if a write request is given a write response signal, to the i_cell_fifo_rd set, 4-byte cell readout from i_cell_fifo, free address and read out from the free address queue (FQ) low 14 are assigned to external SRAM address register (sram_addr), 14 high, sram_addr low 4 position 0. When M_RR is high level, first determines the external SRAM whether there is a read request, if it has a read

request then given a read acknowledge signal, the cell address read out from the queue manager (QC) low 14 assigned to sram_addr high 14, sram_addr low 4 position 0, and the cell address of the high two were assigned to the corresponding head and tail judgment registers, to judge the reading cell whether the head of the packet or the tail of the packet. If neither the external SRAM write request signal nor the external SRAM read request signal come, been waiting for a read or write request signal arrival of status wait_req.

b) wr_ready: MRR negated, the write acknowledge signal is set to low, then read out 4-byte cells from i_cell_fifo and written them into the sram_dout register during status wait_req.

c) wr_ok: Selected external SRAM and write enable can be set to low (low active), bytes from sram_dout would be written into external SRAM, this moment have successfully completed once write operation.

d) wr_judge: If write counter value is less than 15, will i_cell_fifo_rd is set to high, then continue reading cell from i_cell_fifo. If the counter value is equal to 15, no longer read cell from i_cell_fifo.

e) state_judge: i_cell_fifo_rd is set to low, read out 4-byte cell from i_cell_fifo and then them are written into the external SRAM input register (sram_dout), judge whether the write counter value is equal to 15, if equal to 15 then prove a cell of 64bytes have all been written to external SRAM, return status wait_req. If write counter value is less than 15, write counter value plus 1 and return status wr_ok.

f) rd_ready: To the value in the M_RR negated, read acknowledge signal is set to low, select the external SRAM and read enable signal is set to low (low active), read 4 bytes cell from external SRAM and deposited them in the sram_din.

g) rd_o_cell: Bytes from sram_din are assigned to o_cell_fifo_din.

h) rd_ok & judge: o_cell_fifo_wr is set to high, the bytes from o_cell_fifo_din are written into o_cell_fifo. Determines the value of the write counter is less than 15 or not, if the value of the write counter is less than 15, prove that the 64 bytes of the cell have not been completely read out, write counter value plus 1 and skip to status rd_sram, if the value of the write counter is equal to 15, prove at this time the cell has been completely read out, the next step is to jump back to status wait_req.

i) rd_sram: o_cell_fifo_wr is set to low, select the external SRAM and the read enable signal is set to low (low active), read 4 bytes cell from external SRAM and deposit them into sram_din, jump back to status rd_o_cell.

B. Write Control Module

The primarily responsible of write control module is detecting whether the input interface have cell write request, if have cell write request, the write control module will triggers write enable operation of master control module and multicast count module.

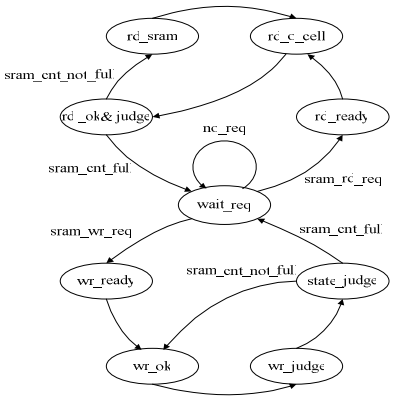

Figure 2. the read and write transition diagram of main control module

The reading and writing process of write control module is shown in Figure 3:

a) wait_i_cell_req: System reset, i_cell_fifo read acknowledge signal is set to low. Determine the i_cell_fifo whether received readout request signal, if there is i_cell_fifo read request signal and the acknowledge signal is low, FQ read enable signal is set to high and read out a free address. If there is no read request signal or the read acknowledge signal of i_cell_fifo is low, then been waiting for the read request signal of i_cell_fifo in status wait_i_cell.

b) wait_FQ_rd: FQ read enable is set to low, if you received the FQ read acknowledge signal, the write enable signal of external SRAM can be set to high, and then wait for the main status machine to enter the write status. If you do not receive a FQ read acknowledge signal, been in the status wait_FQ waiting for the read acknowledge signal of FQ.

c) wait_sram_wr: If you have received the write acknowledge signal of external SRAM, to prove that the main status machine is writing, external SRAM write enable signal is set to low, the write request of the queue manager (QC) and multicast address management (MC) are set to high. If the write acknowledge signal of external SRAM is not received, then been in status wait_sram waiting for the write acknowledge signal of external SRAM.

d) wait_MC_wr: The write request of QC is set to low, if received the write acknowledge signal of MC, then the write request signal of MC is set to low and gives the read acknowledge signal of i_cell_fifo. If the write acknowledge signal of MC is not received, then been in status wait_MC waiting for the write acknowledge signal of MC.

C. Read Control Module

The role of read control module is to detect the QC which has the output weights whether has cell to read out. If there is cell will read out then trigger the Read enable operation of main control module, read out the cell from external SRAM. If the cell has been read out then trigger the read enable operation of multicast counter to judge whether the value of multicast counter is 0.

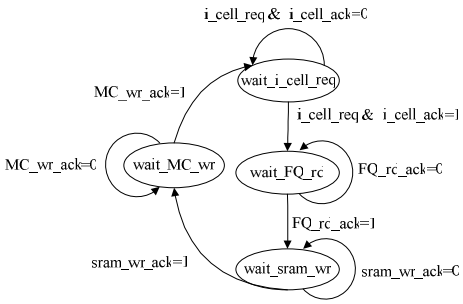

Figure 3. the read and write transition diagram of write control module

The reading and writing process of read control module is shown in Figure 4:

a) wait_qc_rd: FQ write enable signal is set to low. Through polling algorithm (RR) to find the QC which own the output right at this time, if there is QC need output then the read request of external SRAM will be set to high. If there is no QC needs to output, then been in status wait_qc_rd waiting for the output of QC.

b) wait_sram_rd: This means that the main status machine has entered the read status if has received the read acknowledge signal of external SRAM, the read request of external SRAM is set to low, return read acknowledge signal to corresponding QC port and the read enable signal of MC is set to high. If you do not receive the read acknowledge signal of external SRAM, then been in status wait_sram_rd waiting for the read acknowledge signal of external SRAM.

c) wait_MC_rd: The read acknowledge signal of QC is set to low. If received read acknowledge signal of MC, then the read enable signal of MC is set to low. RR plus 1 and detect the pointer returned signal of MC, if received the pointer return signal of MC then the write enable signal of FQ is set to high to recycle the cell address pointer of the output cell, otherwise do not recycle the address pointer of the output cell. If the read acknowledge signal of MC has not been received, then been in status wait_MC_rd waiting for the read acknowledge signal of MC.

d) idle: The write enable signal of FQ is set to low and return to status wait_qc_rd.

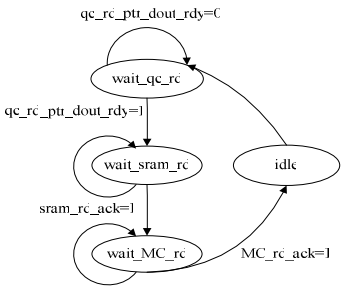

Figure 4. the read and write transition diagram of read control module

D. *Multicast Counting Module*

Multicast counter is realized by a 16K internal RAM, the storage address in the RAM that is the storage address of the cell, the switch fabric has four output ports and each storage space is only 2 bits in size. The system perform the counting operation is according to the storage address of the cell. When cell been written into the switching fabric, system will update the value in the multicast counter according to the multicast fan-out, thereafter whenever the cell is read out, the multicast counter values of this cell are decremented by 1. When the multicast count value of this cell becomes 0, the storage address of this cell will be released back to FQ.

The reading and writing process of multicast counter module is shown in Figure 5:

a) wait_MC_req: System reset. In this state, the first step is to judge whether the MC has a write request signal, if there is no write request signal, then judge whether the MC has a read request signal. If has received the write request signal then go into write status, read acknowledge request is set to high, MC_ram_wr is set to high and FQ output pointer is assigned to MC_ram_addr, the multicast port number of i_cell_portmap is assigned to MC_ram_din which is the input port register of MC_ram. If there is no write request but has read requests, the address pointer of output cell is assigned to MC_ram_addr, and ready to read out the remaining output numbers of the multicast cell. If there is neither write request nor read request come, been in status wait_MC_req waiting for the request signal.

b) MC_wr_ok: The multicast port numbers from MC_ram_din will be write in MC_ram, the write acknowledge signal of MC is set to low and the write enable signal of MC_ram is set to low, then return to status wait_MC_req.

c) MC_rd_out: read out the remaining ports of the output cell and number and deposit them in MC_ram_dout.

d) MC_rd_judge: Give MC the read acknowledge signal, MC_ram_wr is set to high. Once the value of MC_ram_dout is 0, it is prove that the multicast cell has all been read out, return the multicast cell address pointer to FQ. If the value of MC_ram_dout is not 0, then the MC_ram_dout value minus 1 and assigned to MC_ram_din.

e) MC_rd_ok: The data in MC_ram_din is written into MC_ram, the read acknowledge signal of MC and the write enable signal of MC_ram are cleared, return to status wait_MC_req.

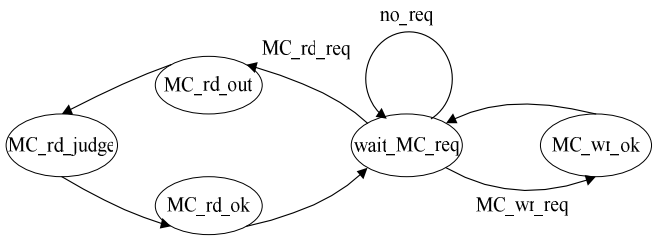

Figure 5. the read and write transition diagram of multicast counter module

III. SIMULATION RESULTS AND ANALYSIS

Xilinx Vertex-5 FPGA is Chosen to achieve the design and implementation of this queue manager, the development environment of this experiment is the Xilinx integrated development environment of ISE13.1. Verilog HDL language is used to achieve this circuit core module, simulation tools is ModelSim SE6.5d, the simulation results show that the circuit functions meet the design requirements.

A. *The Main Control Module Timing Simulation*

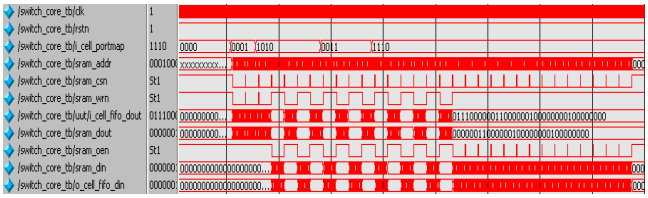

Figure 6. the main control module timing simulation

As shown in Figure 6, the input interface consecutive write four data packets to the switching fabric, the multicast fan-out words are 0001, 1010, 0011 and 1110. Since the external SRAM can only be one-way transmission, so the external SRAM read and write are alternately.

B. *The Write Control Module Timing Simulation*

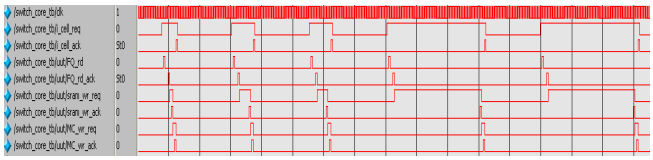

Figure 7. the write control module timing simulation

As shown in Figure 7, when the input interface has cell input request, the system first trigger the FQ to offer the external SRAM memory address to the new cell, and then trigger the external SRAM write request signal to storage the cell, finally trigger the MC write enable signal and record the cell multicast port numbers.

C. *The Read Control Module Timing Simulation*

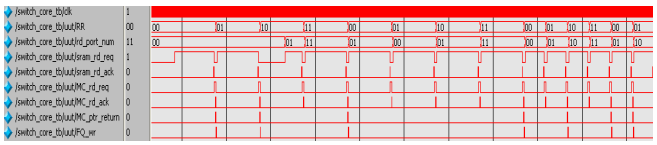

Figure 8. the read control module timing simulation

As shown in Figure 8, the system detect whether the output QC has cell to read out by polling algorithm (RR). If has output, read them from the external SRAM, if has no output, continue to detect the next QC. Triggering the MC read enable signal to detect whether the multicast cell count value is 0 when the cell is read out from the external SRAM, if the value is 0 then recycling the cell storage address.

D. *The Multicast Counter Module Timing Simulation*

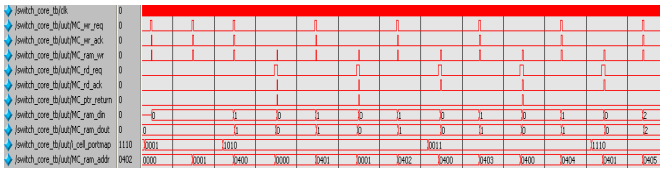

Figure 9. the multicast counter module timing simulation

As shown in Figure 9, the switch fabric sequentially received four packets which multicast fan-out word respectively are 0001, 1010, 0011 and 1110. The MC stored the New-cell multicast count value as soon as it received the write request, whenever the cell is read out once the multicast count of the cell will be decremented by 1. If multicast count value is 0 after the cell was read out, it proved that the cell has been read out completely, so the system will release the cell storage address to FQ.

IV. CONCLUSION

This paper implements a shared memory switching structure with multicast function due to the demand of multicast function on the satellite onboard switch, by address replication method to achieve the multicast function, using multicast counter to manage multicast cell transmission. This multicast circuit structure is simple and applicability. The simulation results show that the cell switching module and multicast counter module can meet the design requirements, with high efficiency. The next step will be the system test to entire switch fabric, detecting the specific delay transmission performance.

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