Optimization of poly-silicon deposition process for switch

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Abstract. Aiming at the severe effect of poly-silicon deposition process on the performance of polysilicon swtich, experiments were made on optimization of poly-silicon deposition and releasing the stress of polysilicon beams to obtain optimal process conditions. By using the optimizing process, the fabrication process for polysilicon mechanical switch is designed, and a poly-silicon micromachined RF MEMS(radio frequency microelectronic machined system) switch has been fabricated. The switch is tested, the results are as follows: the off-state capacitance and on-state capacitance are 0.1 p F and 2.5p F , respectively, and the pull down voltage is 45V. Those optimizing key process technology for fabrication polysilicon mechanical switches is useful, and will be a base for developing RF switch systems with IC.

Introduction

Polysilicon is being extensively used as a structural material in surface micromachining technology for a variety of applications such as pressure transducers, micro-switches, etc. The basic sensing/actuating elements for MEMS are the mechanical microstructures such as beams, bridges, suspended elements, etc. The performance of these mechanical microstructures are critically dependent on the stress releasing process and deposition process [1]-[4]. This paper presents a comprehensive study for obtaining low tensile stress polysilicon beams. The optimizing process technology is that deposition temperature is 580℃, polysilicon films are doped by liquid phosphorus source. Using the optimizing process technology, the single-pole, single-throw poly-silicon micromechanical switch is obtained , it's pull down voltage is 45V. it offers the potential for building a new fully monolithic integrated RF MEMS for radar and communications applications.

Experiments of uniform poly-silicon grains

LPCVD polysilicon is obtained by decomposition of silane (SiH_4) at low pressure in the temperature range of 570-650℃.It is well known that the deposition parameters such as temperature, pressure, and flow rate have a profound effect on the structure and properties of the polysilicon film. The polysilicon films deposited below 580℃ are amorphous whereas those deposited above 600℃ are crystalline in nature. Kamins has observed a similar transition at 600℃ and has suggested that the deposition at this temperature should be avoided in order to obtain reproducible structure[5-8].For obtaining uniform poly-silicon grains, experiments were made on poly-silicon deposition, doping, annealing. Considering that ion implantation and annealing tend to make poly-silicon grain growing rapidly and it is not easy to control the grain size of the poly-silicon, liquid source was adopted for diffusion doping, which could obtain high concentration and also avoid subsequent annealing process. Experiment steps are as follows: starting wafer—oxidation— poly-silicon deposition— observing poly-silicon surface—measuring poly-silicon resistance.

A 2.5μm-thick poly-silicon film was deposited by LPCVD at 610 ℃, with a silane (SiH_4) flow rate of 150 sccm and 50 sccm, and 250 mTorr of vacuum. And then, diffusion doping was made with liquid phosphorous source at 960 ℃ for 1 hour, to obtain a heavily doped poly-silicon film with sheet

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resistance of 2 – 3 Ω/□. Surface of poly-silicon film was observed with a 20X microscope at dark field, as shown in Fig. 1. It has been found that the poly-silicon grain was coarse and big, and the grain size was not uniform. If such heavily doped poly-silicon film was used to make cantilever beams in micro-switches , this cantilever beam is wrapped for high residual stress and stress gradient. Analysis indicated that temperature for poly-silicon deposition by LPCVD was too high, and the poly-silicon obtained more energy for recrystallization, which made poly-silicon grain growing rapidly, and effects of Si-surface contour and non-uniform gas flow during poly-silicon deposition caused local grains to grow faster, and form big grains, resulting poor uniformity of poly-silicon grain size.

In order to reduce the grain size of poly-silicon and improve its uniformity, the temperature for LPCVD was reduced to 580℃ from 610℃, and the poly-silicon film was made between poly-silicon and amorphous silicon. With other conditions unchanged, poly-silicon film with uniform grain size was obtained, which had sheet resistance of 2 – 3Ω/□. Surface of the poly-silicon film was observed with a 20X microscope at dark field, as shown in Fig. 2. It can be seen from Fig. 2 that very few locally crystallized poly-silicon grains could be found, which greatly improved the uniformity of grain size of the poly-silicon film, and thus ensured making poly-silicon cantilever beams for low residual stress.

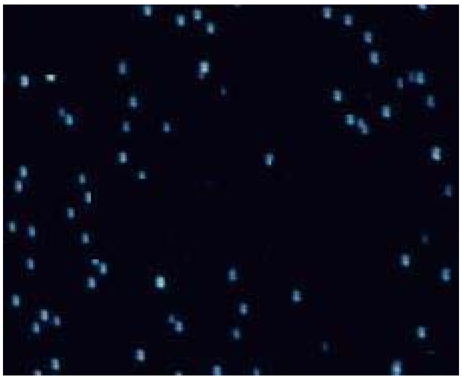

Fig.1 Micro-photograph of poly-silicon film process by 20X micro--scopeat dark field

Fig. 2 Micro-photograph of poly-silicon film using conventional using improved process by 20X microscope at dark field

Experiment of releasing the stress of polysilicon beams

The performance and control of the dimensions of these elements are strongly dependent on the residual stress, and stress gradient in the structural layer, so the deposition and subsequent annealing parameters need to be tailored to obtain films with minimum residual stress and stress gradient [9], and releasing the stress of poly-silicon beams is key process for making the poly-silicon switch. If the residual stress of the poly-silicon beams is big compressive stress, the poly-silicon cantilever is fallen down due to the low restoring force. If the residual stress is high tensile stress, the poly-silicon switch loses the switch function due to the poly-silicon cantilever wrapped. We have presented a simple experiment for obtaining low tensile stress poly-silicon beams. The residual stress of poly-silicon film is dominated by the deposition, phosphorus concentration. Releasing residual stress of poly-silicon has been done by varying the process conditions. The experimental method is as follows, single crystal silicon wafers of <100> orientation and 4″diameter were used as the substrates, a 2.5μm thick LPCVD SiO2 as sacrificial layer is deposited, and liquid phosphorous source is done at 960℃ for 1 hour, the phosphorus doped sacrificial layer is suitable for etching. A 2.5μm thick poly-silicon film is deposited on the LPCVD SiO2 sacrificial layer(the temperature 575,590, 610℃, respectively, at pressures 300—400mTorr in a standard system (Themco Tmx-9000)), and then the poly-silicon film is doped by liquid phosphorous source, a 200μm long and 80μm wide strip is defined by RIE , the sacrificial layer is etched by diluted hydrofluoric acid (48%NH4F: 40%HF:H2O: CH3COOH =5:1:0.5) , only part of the sacrificial layer under the poly-silicon strip is etched by pattern, and then a 100μm long poly-silicon strip is suspended, the poly-silicon suspended beam is formed , whose residual stress varied with conditions under which the poly-silicon beam is formed.

The results are showed in Table 1. From the Table 1, we derived that the residual stress can be released by the optimal process. For high switch speed , the low residual tensile stress existed , so No 5 is the optimal condition. the poly-silicon switch has been developed based on the optimal condition.

Table 1. The change of poly-silicon beam vs conditions under which the poly-silicon beam is formed

NO	Deposition temperature (℃)	Phosphorus doped concentration (x e14,ykev)	Annealing condition (1050℃, xx s)	Phenomena
1	575	1 , 100	10	Wrapped ,and some fell away
2	575	10 , 100	10	Wrapped
3	575	10 , 100	20	Wrapped
4	590	40 , 100	20	no
5	580	100 , 100	40	Weakly wrapped
6	610	10 , 100	20	no
7	610	50, 100	20	no
8	610	10 , 100	40	Fell down
9	610	100 , 100	20	Fell down
10	610	100 , 100	40	Fell down

Experimental results and discussion

On the basis of above optimizing process, the fabrication process for polysilicon mechanical switch is designed, in order to increase the width of polysilicon beams, some $4\times4 um^2$ hole array are etched on the polysilicon beams, the fabrication process is as follows: One micrometer of insulating thermal oxide is grown on the substrate, followed by 0.1μm thick Si_3N_4 is done. A 1μm thick layer of LPCVD poly-silicon is then deposited, followed by phosphorus diffusion is done, the poly-silicon film's deposition and liquid phosphorous source diffusion temperature are controlled for eliminating the local microwelding and reducing hysteresis caused by roughness poly-silicon film, the temperature conditions are 580℃ and 960℃, respectively. The square resistance of the doped poly-silicon layer is 3-5Ω/ , this is necessary for reducing the poly-silicon film resistance. And pattern is defined for the bottom poly-silicon electrode and the input and output terminals. A 0.1μm thick Si_3N_4 is done before the first sacrificial layer, 1 μm thick LPCVD SiO_2 , is deposited, it prevents the bottom poly-silicon and SiO_2 to etch. The hole on bottom contact poly-silicon terminal is made for forming the contact tips for the beam to increase the switching speed and reduce hysteresis, followed by the second sacrificial layer 2.5μm thick, the LPCVD PSG layer, is done. At the input terminal, the contact window is etched, and then the top poly-silicon layer is deposited, which is doped by liquid phosphorous source, followed by the top PSG layer 0.4 μm thick is done. The top PSG layer is then stripped, and the structural poly-silicon is then patterned by etching. The metal interconnection is done by sputtering and patterning. In the last step, the sacrificial layer is partially etched by the optimizing etching process. Using above process steps, the poly-silicon switch with 250μm long, 80μm wide suspended beam has been fabricated, as showed in Fig. 3. The switch is measured by TE2819 capacitance instrument, the off-state capacitance and on-state capacitance are 0.13 p F and 2.5p F , respectively, and the pull down voltage is 45V, as showed in Fig. 3.

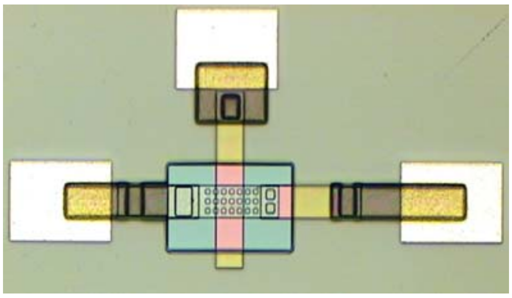

Fig. 3. The micrograph of poly-silicon micro-machined switch

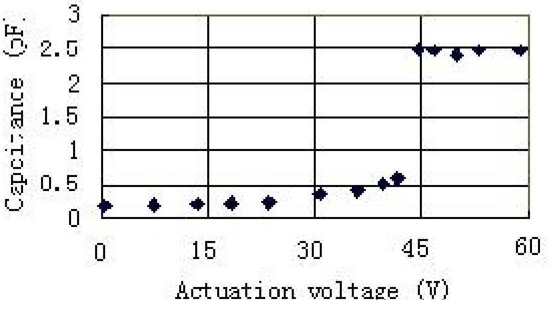

Fig. 4. the curve of capacitance and actuation voltage of the poly-silicon micro-machined switch

The uniform poly-silicon grains deposition and stress releasing technology of polysilicon beams were investigated, and an optimizing process is obtained. The uniform grains of polysilicon films were deposited in the temperature 580℃ at pressures 300—400mTorr, doped liquid phosphorous source, and the low residual tensile stress poly-silicon cantilever is obtained. By using the optimizing process, the fabrication process for polysilicon mechanical switch is designed, and a poly-silicon micromachined RF MEMS(radio frequency microelectronic machined systerm) switch has been fabricated. The switch is tested, the results are as follows: the off-state capacitance and on-state capacitance are 0.1 p F and 2.5p F , respectively, and the pull down voltage is 45V. Those optimizing key process technology for fabrication polysilicon mechanical switches is demonstrated to be useful, and will be a base for developing RF switch systems with IC.

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