

Research on Resonance Soft Switching DC/DC Topologies Used in Cascaded Converters

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Abstract. A new ZVS(zero voltage switching) Push-Pull converter is proposed and compared with other two high efficiency DC/DC topologies. All of them are suitable for the two stage cascaded converter. In order to simplify the circuit and reduce the size, they work in the open loop control mode. Meanwhile, for improving the efficiency, extra resonant inductor and capacitance, or parasitic inductance and capacitance are utilized to realize the soft switching. This paper describes the working principle of the three kinds of topologies, analyzes the conditions to realize soft switching, and gives the design methods. At last, prototypes of the three converters are built, and the efficiency is compared in experiments.

Introduction

In a DC/DC converter which has multiple outputs, wide range input voltage or great voltage difference between input and output voltage, the single stage topology always has the problems such as big voltage or current stress on components, low efficiency, terrible performance, etc. Therefore, the two stage cascaded topology are chosen[1-4]. The first stage topology converts the input voltage into a more stable intermediate bus voltage. Then, the second stage topology converts the intermediate bus voltage into the final output voltage[5]. The two stage cascaded topology can overcome the shortcoming of the single stage topology. It makes the design of each stage topology more flexible. However, efficiency is a key issue needed to be focused on. The efficiency of the two cascaded topology is equal to the product of the two stages. Even if each stage topology can reach 90%, only 81% of the total efficiency will achieve. Since the second stage topology is usually the high efficient POL(Point of Load), how to design high efficiency first stage topology becomes crucial.

A two stage cascaded power supply is built here. The input voltage is 28V and the output voltage are 5V and $\pm 12V$, each output voltage is required to be controlled independently. The total power is 30W. The first stage topology generates an isolated intermediate bus voltage which is lower than the input voltage. Then three independent POLs generate the final output voltages. A new ZVS Push-Pull topology is proposed and compared with the other two candidates.

A New ZVS Push-Pull Topology

The push-pull topology is widely used in the small and medium power DC-DC converter, it has advantages of good magnetic utilization of transformer, simple driving circuit and higher reliability. The relationship between the output voltage and input voltage of the push-pull topology is

$$V_{OUT} = 2 \cdot V_{IN} \cdot D \cdot N. \quad (1)$$

Where, D-the duty cycle of the switch in primary side;

N-the transformer turns ratio.

When the converter works in open-loop, the duty cycle of each MOSFET in the primary side is nearly 50% duty cycle, which makes that $V_{OUT} = V_{IN} \cdot N$ in Eq.1. The output voltage is decided by

the transformer turns ratio. Since the switching device keep on during most time in a period, the secondary side rectifier circuit doesn't need any output inductance to store energy. The output voltage of the converter is affected only by the input voltage rather than the load.

The disadvantage of the push-pull topology is that the MOSFET works in hard switching condition, which reduces the efficiency of the converter. By utilizing the equivalent inductor of the transformer and the output capacitor of the MOSFET, zero voltage switching of the MOSFET can be realized. So the efficiency of the topology is improved. The dead time of the two MOSFETs should be set carefully, when the drain to source voltage of the MOSFET resonate to zero, the gate to source voltage immediately turns high, so the zero voltage soft switching can be achieved.

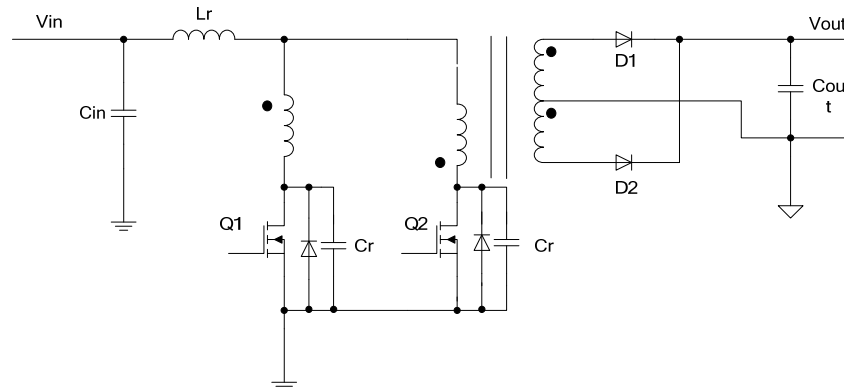


Fig.1 The ZVS push-pull topology

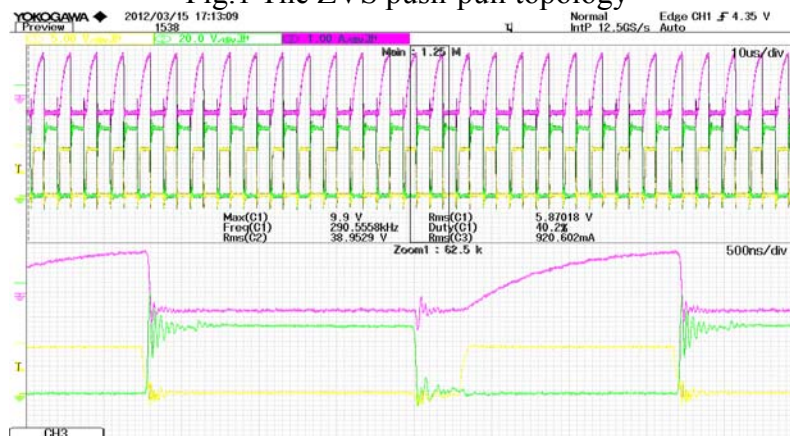


Fig.2 The waveform of drain-gate, gate-source and current of MOSFET

The yellow curve in Fig.2 is the gate-source waveform of MOSFET, the green one is drain-source waveform and the pink one is the primary current waveform. From the figure we see that after the drain-source voltage drops to zero, the gate-source gets to high level to turns the MOSFET on, ZVS is realized.

The dead time should be dependant to the period of resonance. If the dead time is too short, the drain-source voltage of the MOSFET hasn't reached to the zero voltage before the gate-source voltage turns high. On the contrary, if the dead time is too long, there isn't sufficient power transferred to the secondary side, so the output capacitors cannot keep the value of the output voltage.

Zero voltage zero current push-pull topology

The zero voltage zero current (ZVSZCS) push-pull topology is shown in figure 3, the LC resonant tank on the secondary side allows the primary and secondary side current to achieve resonance to realize zero current switching(ZCS) of the MOSFET in the primary side. Using the leakage inductance of the transformer, the added inductor on the secondary side and the junction capacitance of MOSFET, ZVS of the MOSFET in the primary side can be realized.

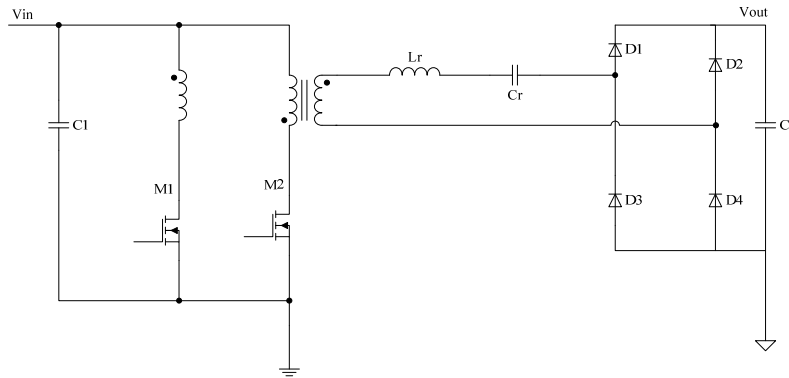


Fig.3 The zero voltage zero current resonant push-pull topology

The corresponding relationship of the resonant frequency and the resonant devices is

$$f_R = \frac{1}{2\pi\sqrt{L_R \cdot C_R}} \quad (2)$$

Where: L_R —the equivalent resonant inductor in the topology,

C_R —Resonant capacitor

In order to make the drain-source voltage resonate to zero within the dead time, we have to ensure that the conduction time of MOSFET is $T_{ON} \geq \pi\sqrt{L_R \cdot C_R}$. Fig.4 shows the experimental waveforms. The yellow curve is the gate-source waveform of MOSFET, the green one is drain-source waveform and the pink one is the primary current waveform. It can be seen that before the MOSFET turns on, its drain-source voltage has resonated to zero, so ZVS is achieved. Before the MOSFET turns off, ZCS is achieved due to the primary side current resonating to zero.



Fig.4 The zero voltage zero current waveform

LLC topology

LLC topology is another topology which is widely used in high efficiency DC-DC converters. It is shown in Fig.5. By setting reasonable parameters of the resonant topology, the MOSFET works in ZVS.

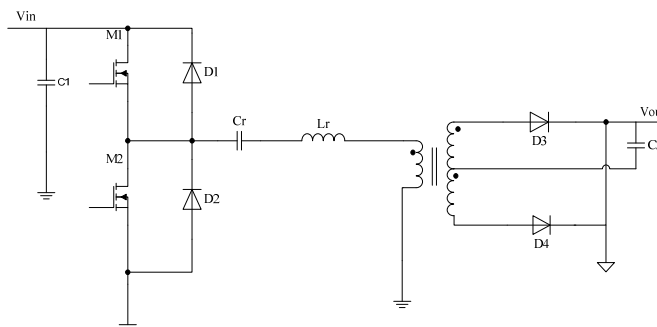


Fig.5 The LLC topology

The experimental waveforms are shown in Fig.6 and Fig.7. The purple curve is the gate-source waveform of MOSFET, the yellow one is the drain-source waveform of MOSFET. Drain-source voltage has been resonated to zero before the gate-source voltage turns high, so the ZVS is achieved.



Fig.6 The waveform of zero voltage switching

The primary side current waveform is shown in Fig.7. The blue curve is the primary side current waveform, the yellow one is the drain-source waveform of the MOSFET. It can be seen that the current lags the voltage applied to the resonant network, which allows the MOSFETs to be turned on with zero voltage. The MOSFET turns on while the voltage across the MOSFET is zero by flowing current through the anti-parallel diode.

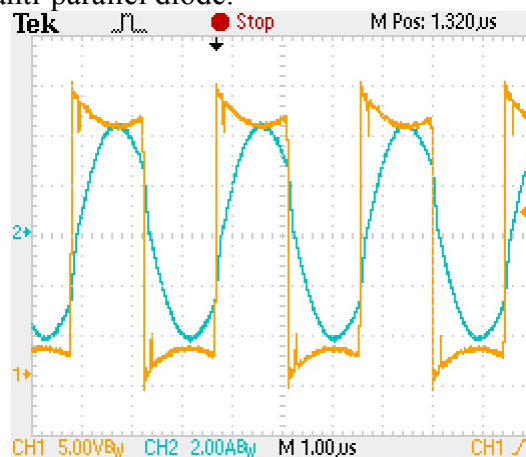


Fig.7 The waveform of zero current switching

Experimental comparison

The three converters analyzed above are all built as the first stage topology, efficiencies are tested under the same working condition. In this application, the input voltage is 28V, the secondary bus voltage is nearly 18V and the output power is about 35W. The resonance parameters have been designed, the MOSFET are IRLR3110, whose on-resistance is 14 m Ω . The rectifier diode is STPS5L60, whose conduction voltage is 0.47V. The output capacitance of IRLR3110 is 180pF. For the topology shown in Fig.1, Only the output capacitor of the MOSFET and the parasitic inductance of the transformer are used to resonate. The turns ratio of the main transformer is 8:6. In the topology shown in figure 3, the resonant inductor and the resonant capacitor of on the secondary side of the transformer is 3.2uH and 88uF. The turns ratio of the main transformer is 8:6. In the topology shown in figure 5, the resonant inductor and resonant capacitor is 1.3uH and 200nF, the main transformer turns ratio is 4:6.

Tab.1 Comparison of efficiency

Topology	Input voltage[V]	Input current[A]	Output voltage[V]	Output current[A]	efficiency
ZVS push-pull topology	27.85	1.438	18.60	1.948	90.5%
ZVS ZCS push-pull topology	27.88	1.337	18	1.756	84.8%
LLC	27.93	1.355	16.38	1.886	81.6%

It can be seen that the switching loss rather than conduction loss dominate in the converters whose input voltage is low and output power is not high.

Although ZCS can be achieved in the ZVSZCS push-pull topology compared to the ZVS push-pull topology, the amplitude of the current waveform is large due to the resonant, which increases the conduct loss. Meanwhile, the extra resonant capacitor and inductor and the MOSFET driving circuit also consume power. The efficiency is further decreased.

Conclusion

Three candidates of the first stage topology in a two stage cascaded converter are analyzed and compared in theory and experiment. It shows that ZVS push-pull topology proposed in this paper has the highest efficiency, the simplest structure, and is suitable for the front stage of the two stage cascaded DC/DC converter in small and medium power.

Reference

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