An on-Chip Clock Controller for Testing Fault in System on Chip

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***Abstract*—In this paper, an on-chip clock (OCC) controller with bypass function based on an internal phase-locked loop (PLL) is designed to test the faults in system on chip (SOC), such as the transition-delay faults and the stuck-at faults. A clock chain logic which can eliminate the metastable state is realized to generate an enable signal for the OCC controller, and then, the test pattern is generated by the automatic test pattern generation (ATPG) tools. Next, the scan test pattern is simulated by the Synopsys tool and the correctness of the design is verified. The result shows that the design of at-speed scan test in this paper is high efficient for detecting the timing-related defects. Finally, the 89.29 percent transition-delay fault coverage and the 94.50 percent stuck-at fault coverage are achieved, and it is successfully applied to an integrated circuit design.**

Keywords: at-speed scan test; on-chip clock; transition-delay faults; phase-locked loop

I. INTRODUCTION

With recent development of semiconductor process, companies that design and manufacture leading-edge products are quickly moving toward very deep submicron (VDSM) integrated circuit (IC) technology [1]. Under the 90 nanometer processing has become the mainstream technology for system on chip (SOC). As nanometer technology has led to a drastic increase in operational frequency, the performance of circuit become more vulnerable to delay variation, testing of SOC has become more challenging [2]. Conventional IC test methodology cannot adequately and cost-effectively test the high clock speed and millions of gates inherent in VDSM technology. At-speed test of IC is becoming critical to detect subtle delay defects [3][4].

At-speed scan test for SOC can test the transition faults and support automatic test pattern generation (ATPG) with Synopsys TetraMAX tool. A key benefit of scan-based at-speed testing is that only the launch clock and the capture clock need to operate at the full frequency of the device under test. And shift data operates at slow speed by slow shift clocks reduce the cost of the test equipment. The automatic test equipment (ATE) which can supply speed clock is often expensive and the ordinary ATE cannot provide the high frequency clock. The design of at-speed scan test in this paper used the internal high speed clock generated by the chip [5][6].

In order to use the approach to test the faults in SOC, additional on-chip controller circuitry must be designed to control the on-chip clocks (OCC) in test mode. The basic idea of the clock control is to use on-chip clock source, such as phase locked loop (PLL) or delay locked loop (DLL), to provide at-speed test pulses, while the ATE provides shift pulses and test control signals at slow speed [7]. But, ATE may not provide at-speed clock to the input pins of device under test (DUT). One issue with using internal PLL clock is that current ATPG tools assume that clock signals are controlled by primary input pins. Therefore, during test pattern generation it is required to modify the circuit model such that clock signals are driven by primary input pins, while during test pattern application on an ATE launch-capture clocks are derived from PLL [8].

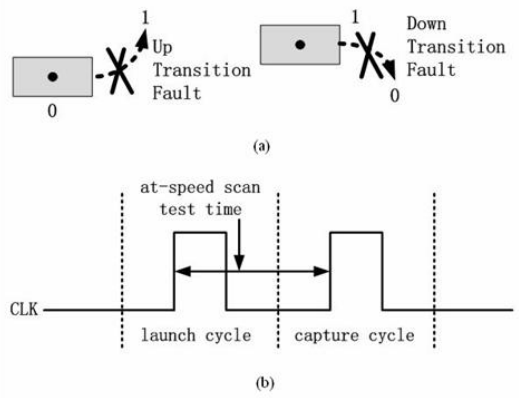

Figure 1. at-speed transition test timing

To detect the path-delay defects in the chip design, the at-speed scan test methodology and the transition-delay fault model were used in this paper. Compared with the traditional method of static faults diagnosis based on the stuck-at faults model, using the transition-delay fault model can detect the slow-to-rise and the slow-to-fall defects in the path by test the stuck-at-0 and the stuck at-1 faults [9]. A slow-to-rise defects means the chip internal nodes state does not correct results from 0 to 1 when the chip runs in high frequency. Similarly, the slow-to-fall defects means the chip internal nodes state does not correct results from 1 to 0 when the chip runs in high frequency, which is shown in Figure 1(a). The ATPG tool generated a launch pulse used the fast clock, and then, it generated another clock pulse used the same clock to

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capture the effect of the launch pulse, and can detect the slow-to-rise and the slow-to-fall faults. Finally, whether the states of the nodes in the chip are correct or not is tested [10]. The time delay between launch and capture cycle is illustrated in Figure 1(b).

II. AN ON-CHIP CLOCK CONTROLLER DESIGN

A. *OCC Controller for At-Speed Scan Test*

When doing test pattern generation for the delay defects, the types of fault models, such as the transition fault model, have been used extensively in industry [11]. To test the transition-delay faults used the fast clock, the PLL logic which can output the clock multiplier in the SOC must be used. And then the OCC controller is used to control the clock to shift and capture the nodes states. Figure 2 shows the design architecture of at-speed scan test.

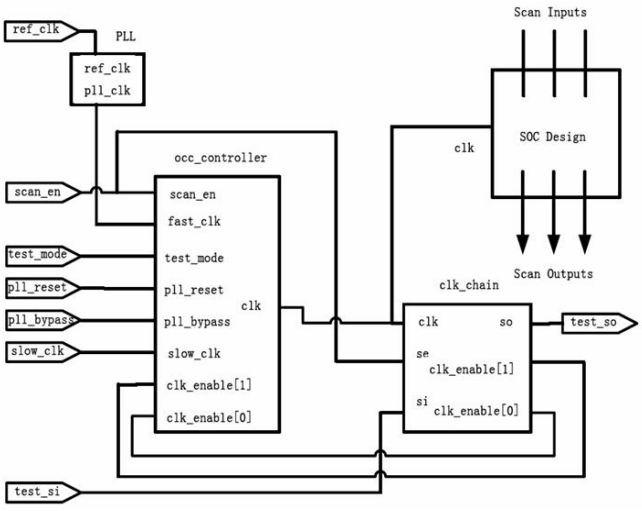

Figure 2. the design architecture of at-speed scan test

The signal function description as follows: The reference clock (ref_clk) is used as a test default frequency input to the PLL circuit and it must be always in free-running state. The PLL clock (pll_clk) or fast clock (fast_clk) is output from the PLL circuit. It is a multiplied reference clock and also works at free-running state. It is used for generating the launch and capture pulse when the scan enable signal is low. The slow clock (slow_clk) is from the automatic test equipment (ATE). So it is also called ATE clock (ate_clk). The slow clock, typically more slowly than a fast clock, is used to shift the scan chain. The ATE clock also drives the reference clock. The internal clock (clk) which is created by the OCC controller circuit is used for driving the scan cells of the SOC design. The test mode signal (test_mode) must be active in order to make sure the circuit is working at testing state. The PLL reset signal (pll_reset) is used once during test setup and initialization. The scan enable signal (scan_en) which must be active during every capture procedure enables switching between the slow shift clock and the fast clock signals. The scan_en signal is used to select between the scan shift operation and the scan capture operation, and also drives the flip-flops scan enable work. The PLL bypass signal (pll_bypass) allows connection of the ATE clock signal directly to the internal clock signals, thus bypassing the PLL clocks.

The OCC controller circuit serves as an interface between the internal scan chains and the clocks which include both fast clock and slow clock. The OCC controller logic typically contains clock multiplexing logic that allows internal clock to switch from the slow clock during shift to the fast clock created by the phase-locked loop circuit during capture. Figure 3 shows the logics of the OCC controller.

The logics of the clock chain, as illustrated in Figure 4, is composed of two special scan flip-flops (DFF0 and DFF1) which are clocked by the falling edge of the internal clock. When the scan_en signal is inactive, the DFF0 and DFF1 work at shift in state. When the scan_en is low, the DFF0 and DFF1 keep up the previous state. The clock enable signals generated by the clock chain logic are used as strobe signal of the OCC controller. The clock output the OCC controller is not emerge burrs or other metastable state because the key of the clock control logic is made up of a series of special shift registers [12].

B. *The design of eliminating metastable state*

Being a part of synchronous circuit, registers could run correctly and reliably if they have no setup and holdup timing violations. However, the design of multi-clock domain is very difficult to guarantee all registers for no timing violations. The timing violations make the registers latch to an inactive level state, which is known as metastable state. The multi-clock domain means the circuit working at two or more different frequency clocks. Some signals which interacted between the fast clock domain and the slow clock domain are known as asynchronous signals. The asynchronous clock domain and the metastable state waveform are shown in figure 5.

The flip-flop in a metastable state will revert to an effective level after the circuit waits some clock cycle. Therefore, we can delay the asynchronous signal by adding some stage registers in the fast clock domain. The registers which are used to delay the asynchronous signal and output a stable signal to the asynchronous clock domain are known as a synchronizer. The two flip-flop synchronizer is illustrated in figure 6. Firstly, the first flip-flop (FF2) delay the asynchronous input signal (data1) from the slow clock domain into the fast clock domain, and then, the asynchronous signal waits for a full fast clock cycle to decay the metastable state, finally, the asynchronous signal is delayed by the fast clock into a second stage flip-flop (FF3). Being the fast clock domain, the asynchronous signal is now becoming a stable and valid signal. If the asynchronous signal via stage-2 flip-flop is still be sufficiently metastable state, it must be clocked into the third stage to eliminate the metastable state.

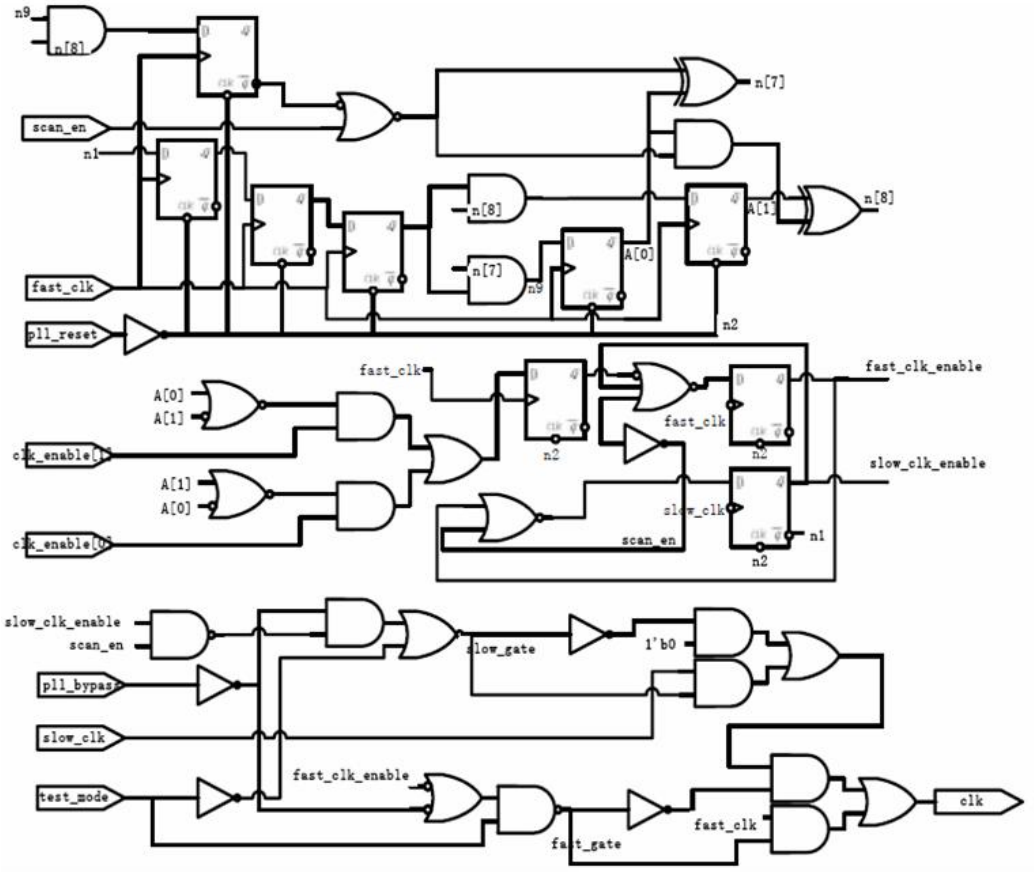

Figure 3. the logics of the OCC controller

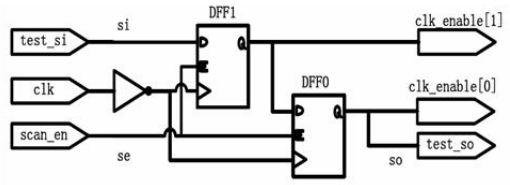

Figure 4. the logics of the clock chain

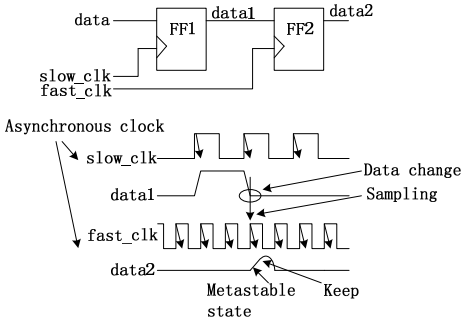

Figure 5. the asynchronous clock domain and its metastable waveform

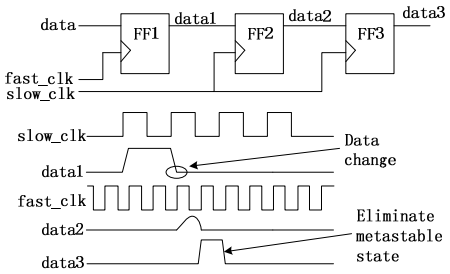

Figure 6. two flip-flop synchronizer

C. *Automatic Test Pattern Generation Flow*

Firstly, the Synopsys Design Compiler tool is used for logic synthesis which is the process of converting the design description written using the Verilog language into an optimized gate-level netlist mapped to a specific technology library and inserting the scan chain to complete the design for testing. The Design Compiler tool can generate a design netlist and a Standard Test Interface Language (STIL) procedure file. The protocol file supports not only the stuck-at test but also the at-speed ATPG test. And then, the

TetraMAX tool, which can obtain information from the STIL procedure file (SPF) needed for test design rule checking (DRC), is used to generate test patterns [13]. Both the stuck-at faults model and the transition-delay faults model are used respectively to generate test patterns in SOC to ensure quality.

The fault coverage of the transition-delay and the stuck-at are achieved as shown in Table 1. Fault coverage can effectively reflect the quality of testing and the calculation formula is shown as Eq.1 [14]. Finally, the 89.29 percent transition-delay fault coverage and the 94.50 percent stuck-at fault coverage are achieved.

$$Fault\_Coverage = \frac{\det ected\_faults}{all\_faults} \quad (1)$$

TABLE I. THE FAULT COVERAGE OF THE TRANSITION-DELAY AND THE STUCK-AT

Fault class (code)	Transition-delay faults	Stuck-at faults
Detected (DT)	1139418	1511761
Possibly deteted (PT)	285	1984
Undetectable (UD)	2896	3349
ATPG untestable(AU)	87661	83362
Not detected (ND)	45976	298
Total faults	1276236	1600754
Test coverage	89.49%	94.70%
Fault coverage	89.29%	94.50%
Patterns	5374	2834

III. CONCLUSIONS

With the PLL performance improvements, the at-speed test method based on the internal PLL structure which is able to detect the timing-path defects is emerged. According to the features of at-speed test, the design for at-speed scan test used the launch-on-shift and launch-on-capture with bypass logic is proposed in this paper. The OCC controller for SOC is designed and the transition-delay faults and stuck-at faults test are realized. The patterns generated based on this architecture have no jitter. Both the transition-delay fault model and the stuck-at fault model are used to test can achieve better yield of SOC chip and the at-speed scan test can be performed using low-cost ATE. The design has high coverage and good universality. Finally, the 89.29 percent transition-delay fault coverage and the 94.50 percent stuck-at fault coverage are achieved, and it is successfully applied to an integrated circuit design.

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REFERENCES

[1] B. Nadeau-Dostie, “Design for At-Speed Test, Diagnosis and Measurement”, Kluwer Academic Publishers, New York, 2002.

[2] T. Yoneda, K. Hori, M. Inoue, et al., “Faster-than-at-speed test for increased test quality and in-field reliability”, IEEE International Test Conference, 2011, pp. 1-9.

[3] V. Iyengar, T. Yokota, K. Yamada, et al., “At-Speed Structural Test For High-Performance ASICs”, IEEE International Test Conference, 2006, pp. 1-10.

[4] I. Pomeranz, S. M. Reddy, “Unspecified Transition Faults: A Transition Fault Model for At-Speed Fault Simulation and Test Generation”, Computer-Aided Design of Integrated Circuits and Systems, Vol. 27, 2008, pp. 137-146.

[5] C. Liang, M. Wu, J. Huang, “Power Supply Noise Reduction in Broadcast-Based Compression Environment for At-Speed Scan Testing”, 19th IEEE Asian Test Symposium, 2010, pp. 361-366.

[6] P. Pant, J. Zelman, G. Colon-Bonet, etc., “Lessons from At-Speed Scan Deplaoment on an Intel Itanium Microprocessor”, IEEE International Test Conference, paper 18, 2010, pp.1-8.

[7] J., M. A. Mateja, J. Wang, etc., “Scan-Based Speed-Path Debug for a Microprocessor”, IEEE Design & Test Computers, 2012, pp. 92-99.

[8] X. Fan, Y. Hu, L. Wang, “An On-Chip Test Clock Control Scheme for Multi-Clock At-Speed Testing”, 16th IEEE Asian Test Symposium, 2007, pp. 341-348.

[9] X. Wen, K. Enokimoto, K. Miyase, etc., “Power-Aware Test Generation with Guaranteed Launch Safety for At-Speed Scan Testing”, 29th IEEE VLSI Test Symposium, 2011, pp. 166-171.

[10] E. K. Moghaddam, J. Rajski, S. M. Reddy, etc., “Low Test Data Volume Low Power At-Speed Delay Tests Using Clock-Gating”, Asian Test Symposium, 2011, pp. 267-272.

[11] Y. Huang, X. Lin, “Programmable Logic BIST for At-speed Test”, 16th IEEE Asian Test Symposium, 2007, pp.295-300.

[12] E. K. Moghaddam, J. Rajski, S. M. Reddy, “At-Speed Scan Test with Low Switching Activity”, 28th IEEE VLSI Test Symposium, 2010, pp.177-182.

[13] P. Pant, E. Skeels, “Hardware Hooks for Transition Scan Characterization”, IEEE International Test Conference, paper 13, 2011, pp. 1-8.

[14] W. Shi, W. Lin, “DFT for the Shadow Logic of Embedded Memory in SOC”, Chinese Journal of Electron Devices, Vol. 35, 2012, pp. 317-321.