Research and Optimization of HDMI Transmitter with Pre-emphasis Strategy

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***Abstract*—Pre-emphasis of LVDS driver for HDMI transmitter (HDMI-TX) is designed and implemented in this paper. HDMI supports high bandwidth and long distance transmission. However, HDMI cable high cost and instability limit its application. Therefore pre-emphasis of LVDS driver is proposed. Compared with traditional LVDS driver, pre-emphasis of LVDS driver can compensate for the high frequency loss. Through research on the encoding method, and clock frequency reduction technology, a FPGA prototype based on HDMI-TX with pre-emphasis is implemented. The simulation shows that the FPGA prototype not only effectively saves energy, but also improves reliability.**

Keywords-HDMI; FPGA; Pre-emphasis; LVDS Driver

I. INTRODUCTION

High Definition Multimedia Interface (HDMI) is the first all-digital interface which supports transmission on a single cable [1], including uncompressed, high-definition, multi-channel audio, intelligent format and control words. Because HDMI can adapt to the bandwidth requirements in the future, it has become the industry standard in consumer electronics.

Through market research, we have found that HDMI transmission cable cost higher than chips. Generally the cable improves the anti-interference and conductive ability using more power conductive mental as the material of the connector and cable, and using Cu grid for electromagnetic shielding. The better quality of HDMI cable can be, the more it costs. But it's still difficult for HDMI cable to achieve 20 meters valid transmission distance. This problem is due to the fact that twisted pair has high-frequency attenuation effect. There exists ISI (Inter-Symbol Interference) when receiving signals [2], which affects the clock and data recovery. It brings a great trouble when bandwidth of the HDMI signal transmission varies from 5GHz to 10GHz or more.

This paper proposes a LVDS (Low-Voltage Differential Signal) driver with pre-emphasis to implement line balancing, which makes long distance transmission and low cost possible.

This paper is organized as follows: in part II, three kinds of encoding period in HDMI transmitter are briefly viewed. In part III, HDMI transmitter with pre-emphasis is explained in detail. Part IV discusses important building blocks of the HDMI-TX. In part V, simulation results is presented and VI makes a conclusion at last.

II. HDMI ENCODING

According to different transmission periods, HDMI encoding can be divided into three periods: 8-bit video data period, 4-bit aux/audio data period, and 2-bit control data period [1].

A. Video Data Period

When VDE (Video Data Enable) equals to 1, transmission period turns to video data period, when VDE equals to 0, it means that video data are invalid. The encoding method adopts TMDS (Transition Minimized Differential Signal) technology as the underlying protocol for HDMI standard.

B. Data Island Period

When control signal ADE (Audio Data Enable) equals to 1, transmission period turns to data island period. The 4-bit aux/audio data are encoded into successive 10-bit word With the TERC4 (TMDS Error Reduction Coding) encoding.

During data island period, zeroth and first bit in channel TMDS0 as two control bits are encoded. The third bit is used to indicate packet header, other channels TMDS1 and TMDS2 are used to transmit data packet.

C. Control Period

During control period, preamble signal is transmitted and provides synchronization between transmitter and receiver. When VDE or ADE is valid, TMDS link should output corresponding preamble and guardband signal before video/audio data are encoded, and preamble signal is used to indicate the data type of upcoming transmission.

If the next transmission period is video data period, control signal outputs video preamble, then outputs video guardband as initial mark before video data is encoded. If the next transmission period is data island period, control signal outputs data island preamble, then outputs data island leading guardband as initial mark before packet data is encoded.

III. PRE-EMPHASIS

A. Pre-emphasis Theory

In serial digital stream, ISI appears when 0/1 is changed after a series of 0 or 1. This phenomenon is due to the capacitance in transmission medium, which is charged or discharged without enough time during the flip moment [2]. Accurate data recovery at receiver becomes impossible.

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Because of conductor and dielectric loss, the transfer function of the HDMI cable becomes a low-pass filter. With equalization techniques, high frequency part can obtain uniform attenuation of frequency response for the system. For the HDMI transmitter, we can compensate for the low-pass property of cable by adopting either following ways. 1. Underactuate a series of the same data artificially. 2. Overdrive the transitional bit artificially, which is called pre-emphasis. After pre-emphasis operation, the ISI effect is usually reduced.

B. *Traditional LVDS Driver*

TMDS technology uses current drive to develop the low-voltage differential signal (LVDS) at the transmitter end of the DC-coupled transmission line [1].

Traditional LVDS driver circuit [3] is shown in Fig. 1. CMOS M5 and M6 constitute current source for the LVDS driver in the form of current mirror. Pin D and $\overline{D}$ are differential signal inputs. OUT1 and OUT2 are outputs. When D=1, M2 and M3 turn on, M1 and M4 are cut off. Current flows from OUT2 to differential cable, and then goes back to OUT1. When D=0, M1 and M4 turn on, M2 and M3 are cut off. The current direction is opposite to the direction of D=1. The receiver reads 0/1 by detecting the voltage polarity of the terminal resistor.

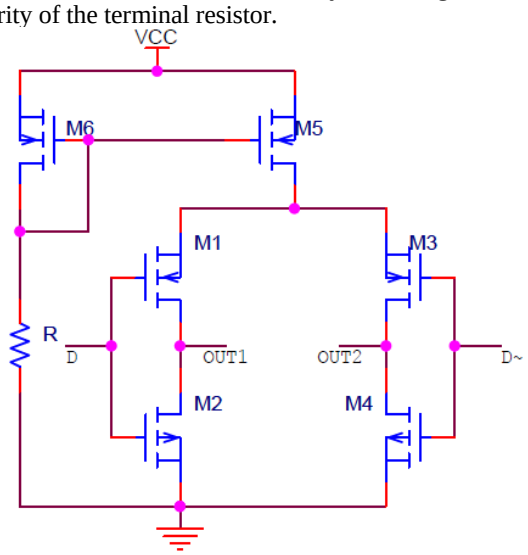

Figure 1. Traditionl LVDS driver circuit

C. *LVDS Driver with Pre-emphasis*

According to the method in [4], an external circuit is added to traditional LVDS driver circuit, and D3, D4, D5, D6 are control signal as shown in Fig. 2. The resistor R represents the load resistor in receiver, node p and n are the LVDS driver output. The above four control signals should satisfy the changing rule below:

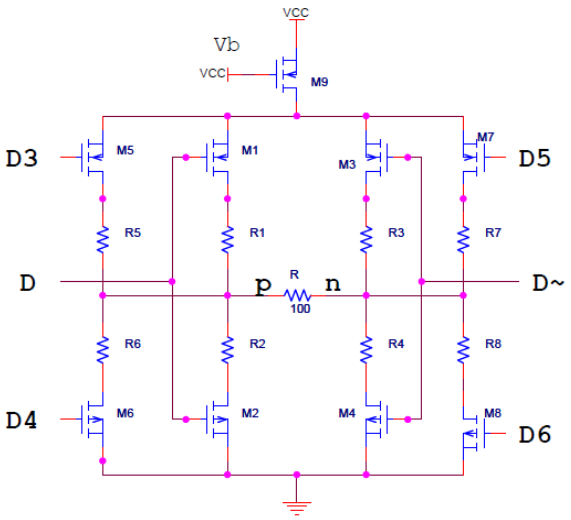

Figure 2. LVDS driver circuit with pre-emphasis

a) When the negative edge of signal D comes, D3 keeps short duration of low-level, and M5 turns on. D6 keeps short duration of high-level, and M8 turns on.

b) When D=0 is stable, we keep D3=1 and D6=0. At this time pre-emphasis is removed.

c) When positive edge of signal D comes, D4 keeps short duration of high-level, and M6 turns on. D5 keeps short duration of low-level, and M7 turns on.

d) When D=1 is stable, we keep D4=0 and D5=1. At this time pre-emphasis is removed.

With the control of D3, D4, D5, D6, the circuit implements pre-emphasis function when the positive or negative edge comes. Once the jump is over, the circuit function is the same with traditional LVDS driver circuit.

IV. MODULE DESIGN

The structure of HDMI transmitter is shown in Fig. 3. Input data consist of 2-bit control signal, 8-bit video data and 4-bit aux/audio data. After encoded into 10-bit word and parallel-serial conversion, the digital stream is loaded to LVDS driver.

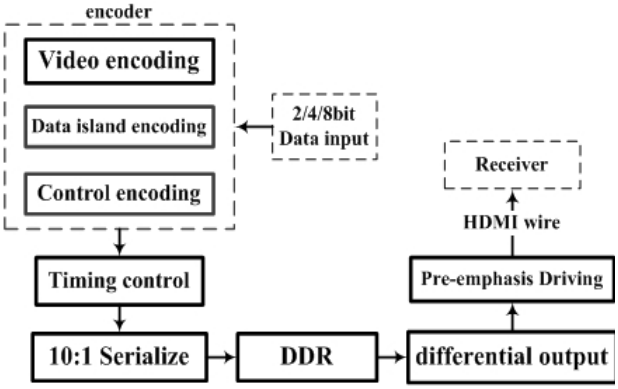

Figure 3. Block diagram of HDMI-TX

A. *Encoder*

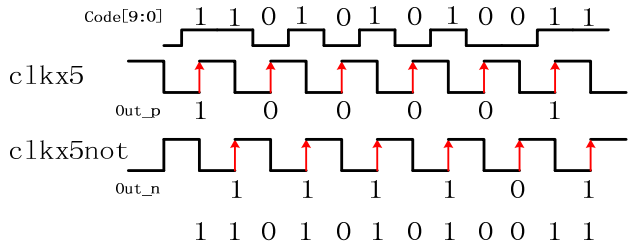

Figure 4. Block diagram of encoder

The structure of encoder module is shown in Fig. 4. Video data, aux/audio data, and control data are fed into encoder, and all the 8/4/2bits data are encoded to 10-bit word under the control of VDE and ADE. The 30-bit encoded word is transmitted by three TMDS links, which are TMDS0, TMDS1 and TMDS2.

For simplicity, the same module of encoder can be invoked by three different TMDS links. The encoder makes full use of the consistency of the channel TMDS1 and TMDS2 in encoding and transmitting, thus it can be used by above two channels. Through identification of TMDS0, encoder module can encode H/VSYNC and packet header etc. which are different from channel TMDS1 and TMDS2.

B. *DDR and Differential Output*

After encoding, 10-bit word is fed into 10:1 parallel-serial converter. The serialization ratio of 10:1 means that converter samples and serially transmits data with the sampling rate 10 times to the pixel clock frequency. This sampling clock is used to implement sampling and serial transmission on TMDS links.

HDTV video with 720p format usually needs bandwidth of 742.5Mb/s; it is difficult for common FPGA to achieve this bandwidth. In order to implement a FPGA prototype and reduce power consumption, we adopt DDR (Double Data Rate) module to make the frequency of sampling clock half of the requirements [5].

In order to produce the sampling clock with five times frequency to pixel clock, we use embedded module-Digital Clock Manager (DCM). DCM can synchronize the pixel clock and produce two phase reversal clocks: clkx5 and clkx5not. After sampling with clkx5 and clkx5not as shown in Fig. 5, all four groups of serial signal, including three channels for 10-bit TMDS data and one channel for clock data are serial output.

The block diagram is shown in Fig. 6. TMDS_P and TMDS_N respectively correspond to the odd bit and even bit of the 10-bit word and the data rate is $5f_{pix}$. After sampling with the clock of clkx5 and clkx5not, the serial data output at the rate of $10f_{pix}$. Through differential output module-OBUFDS embedded in Spartant6, we get serial differential output [5].

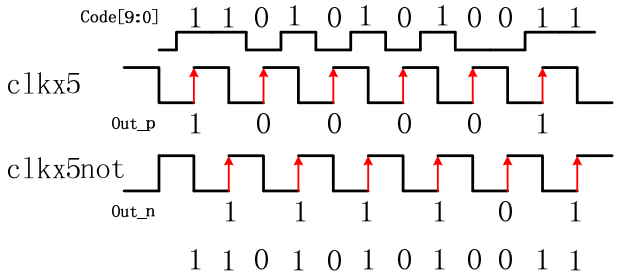

Figure 5. Sampling clock in parallel-serial converter

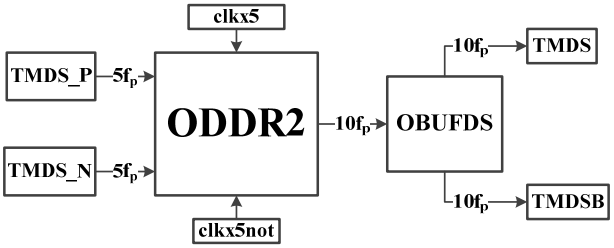

Figure 6. Block diagram of DDR and differential output

C. *Pre-emphasis of LVDS Driver*

In order to coordinate with LVDS driver in Fig. 2, we need to design a digital driver module to implement specific logic functions. In this digital driver module, signal D is input, D3, D4, D5, D6 are output signal. D4, D5 get negation together as soon as the arrival of positive edge of signal D. D3, D6 get negation together as soon as the arrival of negative edge of signal D. After duration of one bit code all control signals get negation again, and the circuit removes pre-emphasis function. Then the circuit keeps working as traditional LVDS driver until another positive or negative edge comes.

V. MODULE SIMULATION

According to different modules functions, we divide HDMI-TX into three modules: encoder module, DDR of differential output module, and pre-emphasis of LVDS driver module. In this section, simulations results of above three modules and the entire HDMI-TX are shown as follows.

A. *Encoder Module*

The behavioral simulation results of HDMI encoder with Modelsim SE6.5 platform are shown in Fig. 7.

In Fig.7, encoder module in HDMI-TX encodes and outputs the preamble, guardband, and video/audio data under the guidance of different control signals. The logic and timing of the output signals are consistent with the HDMI v1.3 standard.

B. *DDR of Differential Output Module*

The module simulation results are shown in Fig. 8. Differential output module implements frequency reduction

and serial transmission. Fig. 8 shows that the differential signal TMDS and TMDSB are the output of entire HDMI-TX. The output can be fed into the pre-emphasis of LVDS driver.

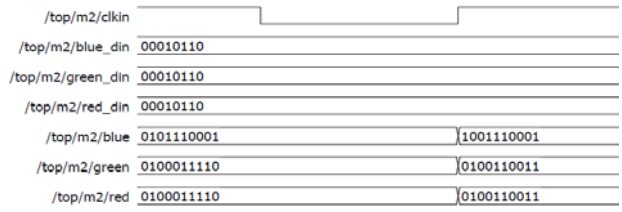

Figure 7. Behavioral simulation with encoder

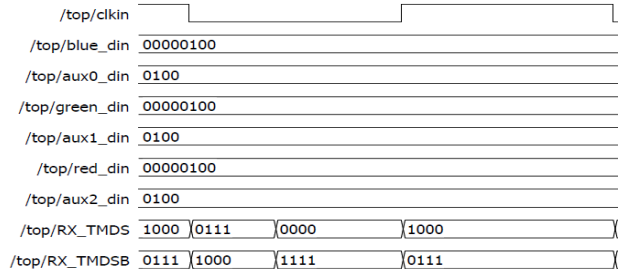

Figure 8. Behavioral simulation with DDR of differential output module

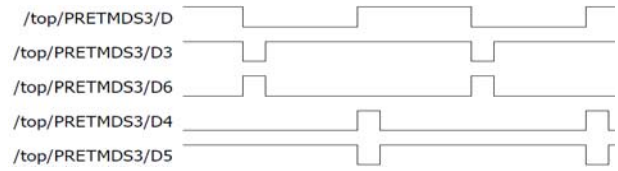

Figure 9. Behavioral simulation with digital driver module

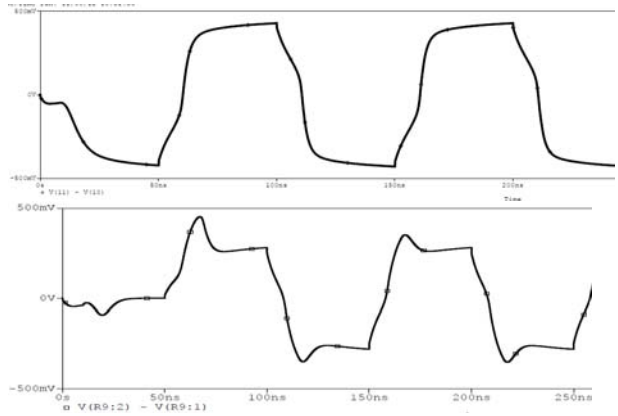

Figure 10. Before and after pre-emphasis of LVDS driver

C. *Pre-emphasis of LVDS Driver Module*

The simulation results of digital driver module are shown in Fig. 9. When the negative edge of signal D comes, D3 gets negative impulse, whereas D6 gets positive impulse. When the positive edge of signal D comes, D4 gets positive impulse, whereas D5 gets negative impulse. Pre-emphasis of LVDS driver is compared with traditional LVDS driver, the simulation is shown in Fig. 10.

In Fig. 10, by output a short pulse at transformational moment the pre-emphasis of LVDS driver can compensate for the high frequency loss, which is caused by low-pass filter from cable.

D. *Synopsis and Post-simulation*

After behavioral simulation with previous modules, synthesis, timing detection and wiring configuration are implemented. Finally it's concluded that post-simulation is the same with behavioral simulation on the whole function.

VI. CONCLUSION

This paper proposes pre-emphasis of LVDS driver for HDMI transmitter to balance energy consumption and reduce the cost of the HDMI transmission. Based on the research on encoding methods and frequency reduction technology, a FPGA prototype is implemented. Simulation results show that this design can reduce the cost and improve reliability in serial transmission.

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