Research on the DFT for Mixed-Signal Circuits

Guo-gang LIAO
Institute of Electronic Engineering
China Academy of Engineering Physics
Sichuan MianYang , China
liaogg06@gmail.com

Jun LI
Institute of Electronic Engineering
China Academy of Engineering Physics
Sichuan MianYang , China
legendiee@sina.com

Chun-yan CHEN
Institute of Electronic Engineering
China Academy of Engineering Physics
Sichuan MianYang , China
ccy307@163.com

***Abstract*—Nowadays with the increases of the density of large scale integrated circuits, researches of Design for Test (DFT) become more and more important. JTAG (JTAG: Joint Test Action Group, also called Boundary Scan) has been widely used in test area, which improves the testability and reliability of mixed-signal circuits. This paper puts forward a scheme to design a test System based on boundary scan technology. The system is realized in an electronic control system, which is composed of mixed-signal circuits. With this method, several test experiments are carried out in the system, which include infrastructure integrity test, interconnect test, cluster test, AD/DA test and so on. The results of experiments show that the system based on JTAG can work normally, which is able to promote the testability of system efficaciously. In a word, the capability of DFT is viable and the system is a virtual tool in the process of DFT design and application.**

Keywords-fault detection;DFT;JTAG; Mixed-Signal Circuits.

I. INTRODUCTION

The most important design for traditional electronic products is realization of the function and test for them is taken into account later[1]. However, with the technical development of large scale integrated circuits, fault detection of high-complexity and high-integration mixed-signal circuits faces with more and more problems than before. Quite a few people think testing as a one of the six "Grand Challenges" for the semiconductor industry within the next 15 years[2].

As a result, researches of Design for Test (DFT) become more and more important. As one of the DFT technologies, Boundary Scan technology has been widely used in hardware testing and software debugging area, which improves the testability and reliability of mixed-signal circuits. Up to now, there are quite a few test devices and correlative software for JTAG designed by many companies such as Corelis, TI, ASSET, etc[3][4]. Otherwise, internal research and application is still backward in comparison with overseas companies.

Boundary Scan technology is one of the most important testability techniques, which have been applied to not only modules and PCB, but also large-scale system. Recently, a great many of researches have been dedicated to the development of creating a trusted a trusted platform based on Boundary Scan. This paper puts forward a scheme to design a test platform based on boundary scan technology, which is realized in a weapon electronic control system.

In this paper, section 1 introduces the foreground and motivation of using Boundary Scan. Section 2 reviews common fault models that are applied for testing. Then on the basis of analyzing of the boundary scan test physical basis, test access port and test structure, correlative test signal standards and test instructions, the system is brought up. Moreover, this paper makes a further step to develop a test platform, which consists of hardware and software based on JTAG. In section 3, several test experiments are carried out with the DFT system, while on the basis of analyzing of the results, this paper concludes in section 4.

II. BOUNDARY SCAN TECHNOLOGY

1990, IEEE Std 1149.1 was published by Joint Test Action Group. Then there are several important modification and broadening for the standard including IEEE Std 1149.4, IEEE Std 1149.6 and IEEE Std 1149.7[5]. Nowadays, it has become popular to provide chips with boundary scan cells and JTAG port, which make it possible that the boundary scan test controller read or write the I/O structures of chips. By this means, fault detection work effectively. Usually, the chips designed based on Boundary Scan technology has Test Access Port (TAP) which comprises 4 or 5 signals[6]. They are test clock input (TCK), test data input (TDI), test data output (TDO), test mode select (TMS), test reset input (TRST, optional). The TAP consists of 16 states and was changed by the level of TMS at the rising edge of TCK. Corresponding to IEEE 1149.1 standard, the boundary scan test instructions comprise EXTEST, IDCODE, BYPASS, SAMPLE_PRELOAD, etc.

Published by Atlantis Press, Paris, France.

III. DFT SYSTEM FOR MIXED-SIGNAL CIRCUITS BASED ON BOUNDARY SCAN

A. *fault models*

1) Logic models

There are three type fault models: logic models, physical models and functional models. Logic models are fault models on the logic level, which are conceivable but not generally applied. Typical electrical fault consists of parametric faults, isolation problem, contact problems, etc.

2) Physical models

Physical models consist of intrinsic failures, electrical stress and extrinsic failures. The group of intrinsic failures subsumes all crystal related defects. Performance degradation is a long-term effect of intrinsic failures. Electrical stress is a continuous source of device defects over product lifetime. It is most often caused by improper handling. Extrinsic failures comprise all defects related to interconnection and packaging.

3) Functional models

Several functional models are shown in table 1

Table 1 Overview of functional models

Fault category	Fault type 1	Fault type 2	Fault type 3
Stuck-at fault	Stuck-at -0	Stuck-at -1	
Bridging fault	AND bridging fault	OR bridging fault	Weak bridging fault
Open fault	Stuck-at -0	Stuck-at -1	

Different fault models may have the same manifestation and some faults do not need specific consideration. Therefore, the faults to be taken into consideration are shown in Table 2.

Table 2 The faults to be taken into consideration

Stuck-at -0	Stuck-at -1	
AND bridging fault	OR bridging fault	Weak bridging fault

B. *DFT system platform*

The design of DFT system platform based on JTAG consist hardware and software.

1) hardware design

The global structure chart of DFT system is illustrated in Fig.1.

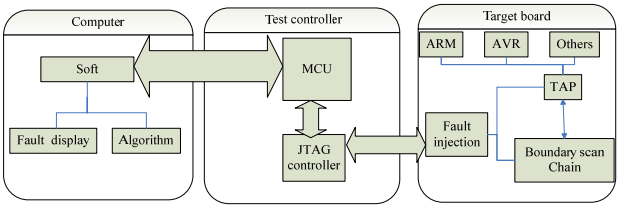

Fig.1 The global structure chart of DFT SYSTEM platform

As shown in Fig.1, the DFT SYSTEM platform based on JTAG mainly consists of an ARM-based target board, a test controller and a PC computer. The soft platform module is mainly designed on the PC computer module including JTAG test algorithm and fault display module. The test controller consists of an AVR chip, JTAG controller and others. The target board is designed for test (DFT) based on a weapon electronic control system, which is composed of mixed-signal circuits including ARM, AVR, etc. It concludes Boundary scan Chain and fault injection circuits. In the test platform, the serial Boundary scan Chain is applied in order to reduce the complexity and improve the reliability. However, there are few problems in common serial Boundary scan Chain. For instance, it is difficult to find the location of fault exactly. The enhanced serial Boundary scan Chain solves the major problems, which is illustrated in Fig.2.

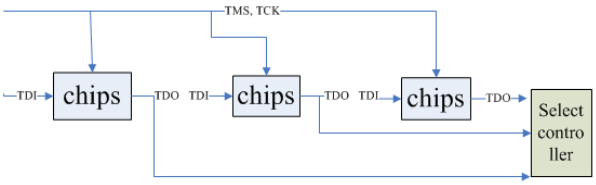

Fig.2 The enhanced serial Boundary scan Chain

2) software design

It is very important to choose the best test algorithm and designing a suitable controlling program design for JTAG test. As a result of the high fault coverage rate and nice testability, Walk “1” algorithm is selected. The flow chart of controlling program design is illustrated in Fig.3. The order of writing or reading JTAG controller register by MCU is key of point.

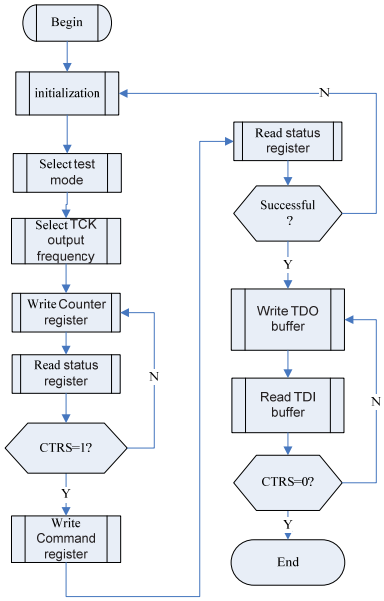

Fig.3 The flow chart of controlling program design

In short, the DFT system platform reads net list files and BSDL (Boundary Scan Description Language) of the

mixed-signal circuits, analyzes the structures of them and generates the test patterns for experiments. The test patterns are described as SVF (Serial Vector Format) according to the international industry standard and generated based on Walk "1" algorithm. Then several fault injection experiments are carried out in the DFT system platform, which includes integrity test, interconnect test, cluster test and so on. The results are analyzed to test and verify the availability of the DFT system platform.

IV. RESULTS

The results of fault injection experiments are illustrated in table 4.

Table.1 The results of integrity test

number	test patterns	respond patterns	expect results	practical results
1	10000001	10000001	No fault	No fault
2	10000001	11111111	open fault	open fault

Table.2 The results of interconnect test

number	test patterns	respond patterns	expect results	practical results
1	100 010 001	100 111 001	The 2nd line stuck-at-1	The 2nd line stuck-at-1
2	100 010 001	100 000 001	The 2nd line stuck-at-0	The 2nd line stuck-at-0

Table.3 The results of cluster test

number	test patterns	respond patterns	expect results	practical results
1	100 010 001	011 101 110	No fault	No fault

From the above tables, it can be concluded that integrity test, interconnect test, cluster test is achieved and most of fault models are detected successfully.

V. CONCLUSIONS

The results of experiments indicate that the DFT system based on JTAG can work normally, which is able to detect stuck-at faults, open faults and bridging faults on board, and additionally can reduce effectively the complexity of test. In a word, the capability of DFT system is viable and the system is a virtual tool in the process of DFT design and application. However, the experiments are not exact and adequate entirely, more experiments will be carried out and better DFT system platform (including hardware and software) will be designed in the future.

ACKNOWLEDGMENT

The author especially wishes to thank Li Jun for his comments, for reviewing and contributing to the design methods. The author also especially wishes to thank Chen Chun-yan for her comments, technical suggestions, which contribute to the hardware and software design. The author also wishes to thank Suo Bing, Ye Hong and other colleagues for their review and useful suggestions.

REFERENCES

[1] Tehranipour M H , Ahmed N, NouraniM. Multiple transition model and enhanced boundary scan architecture to test interconnect s for signal integrity [C].Computer Design. San Jose, C A , USA : IEEE ,2003 :554 – 559

[2] Quiros-Olozabal & M. A. Cifredo-Chacon, A New Algorithm for the Selection of Control Cells in Boundary-Scan Interconnect Test [J]. Electron Test, 2009; 25:187–195.

[3] Niu Chunping, Ren Zheping, Five modified boundary scan adaptive test generation algorithms [J].Journal of Systems Engineering and Electronics , 2006.4: 760 -763

[4] Martin Kutz, The complexity of Boolean Matrix Root Computaion [J].Theoretical Computer Science.2004, 325(3):373-390

[5] IEEE.IEEE Std.1149.6-2003: IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks[S]. April,2003 ; 6:1-53

[6] Keunyoung Park & Sang Guun Yoo & Taejun Kim & Juho Kim, JTAG Security System Based on Credentials[J]. J Electron Test, 2010; 26:549–557