A Hardware/Software Testbed for the Design of OFDM Systems

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***Abstract*—A field programmable gate array (FPGA)-based hardware/software co-verification scheme is proposed for the design of orthogonal frequency-division multiplexing (OFDM) baseband systems. It provides a platform to simulate the software implementation and verify the hardware implementation of a baseband OFDM system. The baseband system is divided into two partitions implemented by software and hardware respectively. User datagram protocol (UDP) is used for data transmission to connect these two partitions via Ethernet, and hence integrates the complete baseband system. A radio-frequency (RF) front-end is also provided to modulate baseband signals and demodulate RF signals. Therefore, the software simulation in the testbed is running over real wireless channels, which can verify the correctness of the algorithm. On the other hand, the hardware implementation can be verified by software processing in real time, which makes the fault localization more efficient. An example of equalizer design is introduced to illustrate the effectiveness of the proposed testbed.**

Keywords-FPGA; OFDM; baseband system; testbed

I. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) transmission scheme has been widely used in wireless communications such as digital broadcasting, wireless local area network (WLAN) due to its high spectral efficiency and the ability to overcome multipath fading [1]. Since there are many functional modules within an baseband OFDM system and the modules need to be tested under wireless environment, it is not an easy task to implement the baseband OFDM system with the application-specific integrated circuit (ASIC). Therefore, a scheme for evaluating the performance of algorithms and verifying the functional correctness of modules is important for the implementation of baseband OFDM systems.

System simulations implemented in high-level languages such as C and C++ are efficient and flexible to debug and modify [2]. However, the pure software simulations cannot take fully account of impairments encountered in realistic environment such as channel fading, carrier frequency offset, etc. The actual performance of the implemented algorithms, therefore, cannot be guaranteed. The hardware verification is an important step in ASIC design. With the test on field-programmable gate array (FPGA) under realistic environment, the correctness of modules can be verified effectively [3]. The disadvantages of hardware verification are high operational complexity, low flexibility, and the difficulty in fault localization. Although many FPGA vendors provide on-chip debugging tools like the Altera SignalTap II Logical Analyzer [4], the sample storage is limited by the size of random access memory (RAM) on FPGA, and it is difficult for those tools to process the samples with other software applications in real time.

Considering the advantages of software simulation and hardware verification, the paper proposes an FPGA-based hardware/software testbed for the design of baseband OFDM system. The baseband system is divided into two parts, which are implemented in C/C++ and hardware description language (HDL), respectively. The platform connects these two parts with Ethernet and establishes the whole system. With the help of the testbed, software simulations for the evaluation of algorithms can run over real channel, and the results of HDL modules can be processed immediately at the software partition, which makes the fault localization of HDL designs more efficient.

The rest of the paper is organized as follows. Section II introduces the model of a baseband OFDM system. Section III presents the hardware/software testbed in detail. Section IV gives an instance of the equalizer design to demonstrate how the testbed works. Finally, conclusions are drawn in Section V.

II. BASEBAND OFDM SYSTEM MODEL

In an OFDM system with N carriers, from $t=t_s$, the baseband signal can be described as

$$s(t)=\sum_{i=0}^{N-1} d_i \,\mathrm{rect}\left(t-t_s-\frac{T}{2}\right)\exp\left(\mathrm{j}2\pi\frac{i}{T}(t-t_s)\right) \quad -\infty\le t\le+\infty, \tag{1}$$

where T is the OFDM symbol duration, and d_i (i=0,1,⋯,N–1) represents the data symbol assigned to the ith subcarrier. The function rect(·) is the rectangular window, which is rect(t)=1, $|t|\le T/2$.

Let T/N be the sampling rate of s(t). From $t=t_s$, the discrete signal can be expressed as

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$$s_k = \sum_{i=0}^{N-1} d_i \exp\left(\mathrm{j}\frac{2\pi ik}{N}\right) \quad 0 \le k \le N-1. \qquad (2)$$

Equation (2) shows that the OFDM signal s_k can be obtained by the inverse discrete Fourier transform (IDFT) of d_i. Therefore, the transmitted data d_i can be recovered by the discrete Fourier transform (DFT) at the receiver. In addition to DFT/IDFT modules, some other modules are required to improve the overall performance of the baseband OFDM systems. Channel codec helps correct errors during transmission. Digital modulation such as phase-shift keying (PSK) or quadrature amplitude modulation (QAM) provides higher data rates. The cyclic prefix (CP) is exploited to eliminate inter-symbol interference (ISI). Synchronization and channel equalization are designed to recover transmitted frames at the receiver. A typical diagram of a baseband OFDM system is shown in Fig. 1. Some other modules are not plotted for space constrains. For example, scrambling converts a data bit sequence into a pseudorandom sequence that can eliminate long strings of 0s or 1s; interleaving spreads out burst errors and enhances the performance of channel codec.

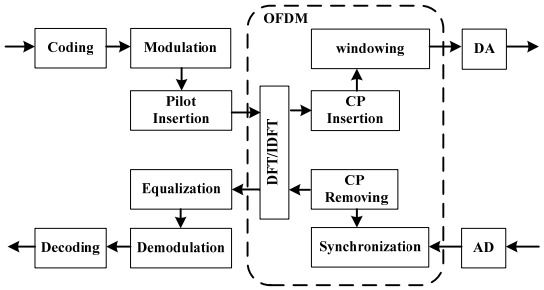

Figure 1. The baseband OFDM system model

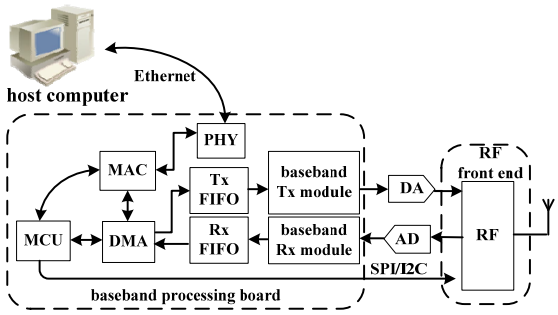

Figure 2. The architecture of the testbed

III. HARDWARE/SOFTWARE TESTBED

The design of an OFDM system includes many functional modules as analyzed in Section II. This section introduces a testbed to simulate and verify the baseband OFDM system, as shown in Fig. 2. The platform is composed of two partitions: hardware and software. The hardware partition contains the baseband processing board and the radio-frequency (RF) front-end. The software partition consists of the baseband software modules and the scheme of user datagram protocol (UDP) data transmission between computer and FPGA.

A. Baseband processing board

The baseband processing board is the primary module in the testbed, as is shown in Fig. 2. It enables a full-duplex communication with host computer via the Ethernet physical layer (PHY). The analog-to-digital converter and digital-to-analog converter (AD/DA) are used for the connection with the RF front-end. Several functional intellectual property (IP) cores are integrated on FPGA for the verification, including micro control unit (MCU), Ethernet media access controller (MAC), direct memory access (DMA) controller, transmit and receive first-in-first-out buffers (Tx/Rx FIFOs), and baseband HDL modules of OFDM systems (baseband Tx/Rx modules) under test.

MCU, an 8-bit microprocessor compatible with the 8051 instruction set, is the system controller operating at 16 MHz. It manages DMA for data transmission between MAC and FIFOs, configures RF front-end via serial peripheral interface (SPI) or inter-integrated circuit (I2C) bus, and implements upper-layer protocols for the Ethernet transmission.

MAC connects the Ethernet PHY via media independent interface (MII). It implements the functions of carrier sense multiple access with collision detection (CSMA/CD) and 32-bit cyclic redundancy check (CRC).

DMA is used for the high-speed data transmission between MAC and FIFOs. Since the operating frequency of MCU is limited, only the headers of Ethernet packets are processed by MCU, whereas the data of Ethernet packets are transmitted by DMA. For example, when the data in Rx FIFO are transmitted to host computer, MCU prepares the header of a packet, and then DMA sends the data of the packet from Rx FIFO to MAC.

The Tx/Rx FIFOs are buffers for the data samples from the baseband Tx/Rx modules. Both of the FIFOs are asynchronous FIFOs, because the operating frequencies of the baseband Tx/Rx modules depend on the HDL design under test, whereas the operating frequency of DMA is always the same with MCU.

The baseband Tx/Rx modules are some functional HDL models for OFDM systems. These two modules are the designs under test. A whole baseband OFDM system in Fig. 1 is constructed in these two modules and the software baseband modules on the host computer.

B. RF front-end

The RF front-end realizes the conversion between baseband signals and RF signals. It consists of local oscillator, RF modulator/demodulator, power amplifier, low noise amplifier, etc. With the help of the RF front-end, the performance of a software algorithm as well as its hardware implementation can be verified under the real wireless environment. The parameters of the RF front-end, such as

carrier frequency, transmit power, etc., are configured via SPI or I2C.

C. UDP data transmission

In the testbed, the connection between software baseband modules on FPGA and hardware baseband modules on host computer is realized by Ethernet. The connection is established by the client-server architecture, where the computer and the FPGA are client and server respectively.

UDP as a kind of transport layer protocol provides an unreliable and connectionless communication service. This means UDP is effective to real-time application where low latency and low delay are preferred, and therefore, is suitable for simple and fast data transmission between software and hardware baseband modules [5]. Fig. 3 demonstrates a timeline of the scenario that appears in a UDP client/server exchange. Although UDP has no flow control, the application here is built with request-reply model to provide a more reliable transmission. At the very beginning, both the client and server start with a call to socket. The server then calls the bind which assigns a local protocol address to a socket. At client/server sides, the 'recv' operation is used for receiving datagram, whereas the 'send' operation is responsible for sending datagram. During the transmission process, the lost packets can be detected using a retransmission timeout mechanism which allows the client retransmits the request to the server if a reply fails to be received. The mechanism is also available during the baseband data transmission. Fig. 3(a) shows the transmitting process in which the baseband data are transferred from the client to the server. Fig. 3(b) shows how the server sends the sampled baseband data to the client after a request.

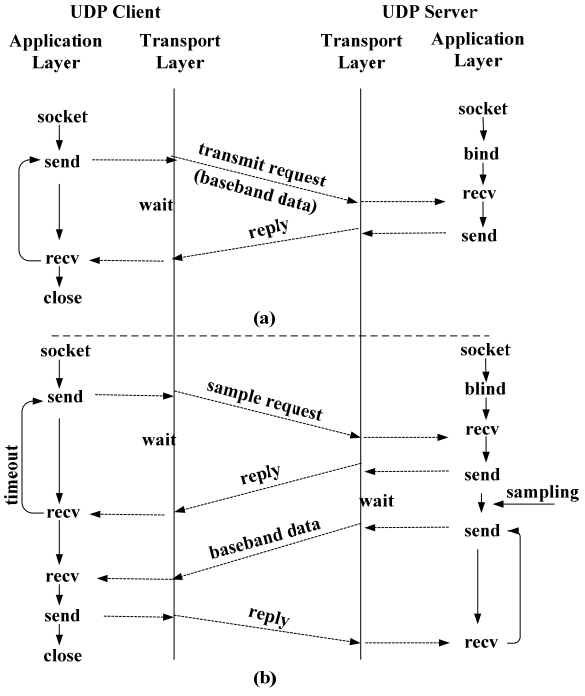

Figure 3. UDP data transmission mechanism

D. Baseband software module

Baseband software modules are some functional models in C/C++ for OFDM systems. These software modules on host computer are used for the simulation of algorithms in baseband OFDM systems. Software simulation, as the first step in hardware designs, can verify the correctness and effectiveness of algorithms. After the algorithm is verified to be proper, it will be implemented in HDL. Since the testbed runs over the real wireless channel, the algorithms under test can be evaluated with the effect of channel fading, carrier frequency offset, sampling frequency offset, etc. Therefore, the testbed provides an integrated platform for the software simulation and the hardware verification of baseband OFDM systems.

IV. Application to Equalizer Design

In OFDM systems, due to the effect of frequency offset, channel fading, etc., the receivers have to make some effort to recover the transmitted data. In this section, the design of an equalizer is set as an example to illustrate how the proposed testbed works for the design of a baseband OFDM system.

The FPGA is Altera Cyclone IV EP4CE115. AD/DA has a sampling rate of 20MHz with 12-bit resolution. The RF front-end is designed for the carrier frequency 2.4 GHz. The OFDM frame structure refers to the IEEE 802.11a frame format [6]. It consists of 10 sets of 16-point short training sequences, 32-point guide interval, 2 sets of 64-point long training sequences, an 80-point BPSK-based Signal segment and a series of 80-point Data segments. In this simulation and verification, 22 sets of Data segments are sent in each OFDM symbol with 16QAM modulation. Additionally, 411 sampling points are arranged between every two frames. The testbed is shown in Fig. 4.

For the simulation and verification of the equalizer, the HDL models of synchronizer and fast Fourier transform (FFT) have been implemented on FPGA.

Assume that the channel is time-invariant frequency-selective. Then the channel coefficient of the kth sub-carrier can be denoted by H_k. Let $\mathbf{X}_{\mathrm{LT}}$ and $\mathbf{Y}_{\mathrm{LT}}$ represent the transmitted and received long training sequence in frequency domain, respectively. The channel coefficient can be estimated by the least-square (LS) algorithm [7] as

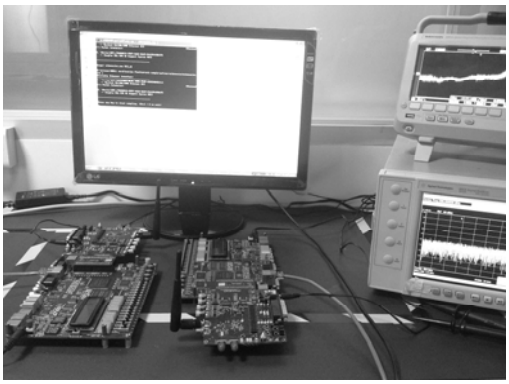

Figure 4. FPGA-based hardware transceiver of OFDM system

$$\hat{H}_k = \frac{\mathbf{Y}_{\mathrm{LT}}(k)}{\mathbf{X}_{\mathrm{LT}}(k)}. \quad (3)$$

Therefore, with the received OFDM symbol **Y**, the LS estimation of the transmitted data is

$$\mathbf{X}(k) = \hat{H}_k \mathbf{Y}(k). \quad (4)$$

Fig. 5(a) shows the software simulation of the equalization. A received frame is synchronized in the baseband processing board. Then the data including the long training sequence are transformed to the frequency domain. The results of FFT are sampled and sent to host computer. The software equalizer implemented in C/C++ processes the samples and analyses the performance such as the bit error rate. Fig. 6 shows the constellations of the results of received frames. It shows that the equalizer compensates for the effect of channel fading effectively.

After the equalization algorithm is validated by the software simulation, the next step is to implement the equalizer in HDL. The HDL model of the equalizer is also verified in the testbed. Fig. 5(b) shows the diagram of hardware verification for the equalization module. If the

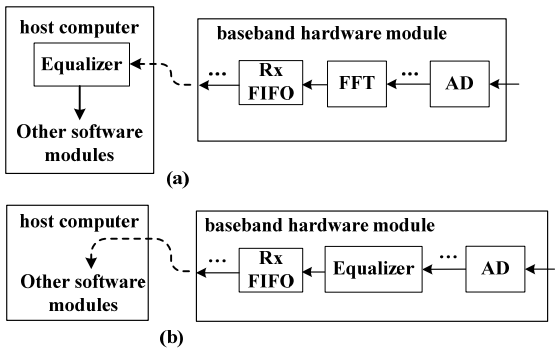

Figure 5. Block diagram of equalizer verification: (a) Software simulation (b) Hardware verification

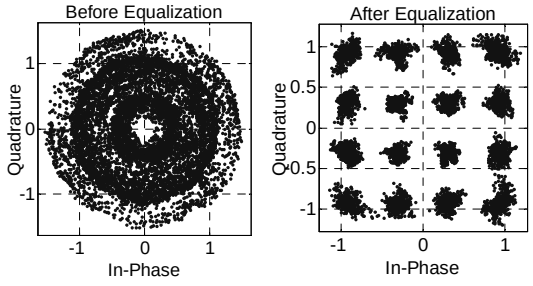

Figure 6. Constellations of 16QAM modulation before and after equalization

HDL model of the equalizer is correct, the constellation results will be the same as the software model.

In this way, other functional modules of the baseband OFDM system can be designed and verified, and consequently a hardware OFDM system can be established.

V. CONCLUSIONS

A hardware and software joint testbed has been proposed for the design of baseband OFDM systems. The platform splits the baseband system into software partition on host computer and hardware partition on FPGA. It uses Ethernet to connect these two partitions to establish an integrated OFDM system. Since the proposed testbed runs over real wireless channels, it provides a uniform environment for the software simulation and hardware verification. In addition, the testbed is portable for the design of other wireless baseband systems, as long as the RF front-end is redesigned for the target application.

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