

# Run-time Leakage Reduction in Near-threshold Circuits with Gate-length Biasing Techniques

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**Abstract**— In this paper, we investigate the low leakage design method for near-threshold circuits with gate-length biasing techniques. A cost-effective gate length optimization method is presented. The basic logic gates and two full adders with gate-length biasing technique are implemented and simulated using HSPICE at 45nm CMOS process. The simulation results show that the proposed gates achieved considerable leakage reduction.

**Keywords**— low power; leakage reduction; gate-length biasing; near-threshold computing

## I. INTRODUCTION

With the integrated circuits process technology progress, power dissipation has become the main concerning in today VLSI design. There are three main components of power dissipations in CMOS chips, namely, short-circuit dissipations, dynamic dissipations and leakage power dissipations. In sub-micro CMOS process, dynamic energy loss is the most main power dissipation in CMOS circuits. Therefore, the conventional approaches to achieve low-power design are to reduce the supply voltage, the loading capacitances of gates, and the switching activity [1]. However, the most effective way to reduce the power consumption is to lower the supply voltage of a circuit, because of the square relationship between power dissipation and supply voltage. Sub-threshold logic with the supply voltage below the threshold voltage of the MOSFET has shown significant improvement in the term of power consumption [2]. While, there are some pitfalls in the sub-threshold logic such as large performance and robustness degradation, more sensitive to process variation etc. [2-3].

Recently, the near-threshold computing is presented. The supply voltage of near-threshold circuits is slightly above the threshold voltage of the transistors. This region retains much of the energy savings of sub-threshold operation with more favorable performance and variability characteristics. The research results from Dejan M. et al. shown that a 20% increase in energy from the minimum-energy point gives back tens times in performance [4]. This makes it applicable for a broad range of power-constrained computing segments from wireless sensors to biomedical applications.

With the scaling of CMOS technology, the power dissipation caused by leakage current can consume upwards of half of the total power consumption of modern high-performance VLSI chips. There are three major leakage currents in a MOSFET: sub-threshold leakage current, gate

leakage current and band-to-band tunneling leakage current. Leakage-reduction methodologies can be divided into two classes: standby techniques and runtime techniques. Several standby leakage reduction techniques have being proposed, such as dual threshold CMOS, variable threshold CMOS, input vector control, and stacking transistor technique, power gating technique, etc. [5]. The runtime leakage reduction techniques include multi- $V_{th}$  manufacturing process and gate-length biasing [6-7].

Gate-length biasing is a promising technique due to the fact that it requires no extra process and can be performed at any stage in the design process. However, the previously studies focus mainly on the nominal supply voltage. In near-threshold circuits, there still exists the leakage dissipation. There are many different characteristics of the MOSFET devices operation in near-threshold region compare with that in super-threshold region. In this paper, we investigate the leakage currents of MOS devices operation in near-threshold region at 45nm technology nodes. A cost-effective gate-length biasing technique for near-threshold circuits is presented.

The organization of this paper is as follows. In Section II, the near-threshold computing is introduced. Section III, we describe the proposed gate-length biasing methodology for leakage reduction. Section IV presents the experiments and results for the validation of the proposed ideas. The conclusion is dedicated at last.

## II. NEAR-THRESHOLD CIRCUITS

Near-threshold logic circuits with the operation voltage slightly above the threshold voltage of MOS transistors provide one of the best tradeoffs between power consumption and performance in low power applications [4].

The energy and delay relationship with scaling of the supply voltage ( $V_{dd}$ ) should be demonstrated using a variable activity factor ring oscillator characterization circuit. The circuit consists of an 11-stage 2-input NAND ring oscillator with 9 additional 11-stage NAND delay chains driven by the ring oscillator, as shown in Figure 1. The Select inputs to the delay chains can be used to “activate/deactivate” different delay chains. Then the activity factor of the circuit from 0.1 to 1 can be achieved.

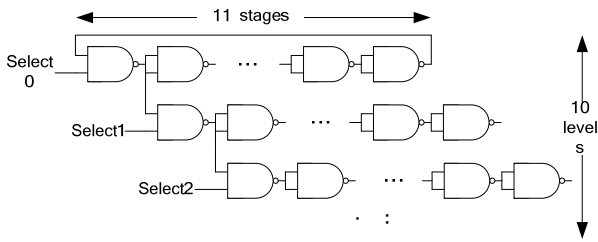


Figure 1. Circuit to show energy and performance for variable activity factor.

With the supply voltage varying from 0.1V to 1.1V, the energy and delay of the NAND2 ring oscillator in different activity factors is simulated using HSPICE at a 45nm CMOS process with the PTM (predictive technology model) BISM4 model. The threshold voltage of PMOS and NMOS transistors is -0.423V and 0.471V, respectively. The device size of PMOS and NMOS transistors of the NAND2 is taken with  $W/L = 8\lambda/2\lambda$  and  $W/L = 4\lambda/2\lambda$ ,  $\lambda = 25\text{nm}$ , respectively. The simulation results are shown in Figure 2.

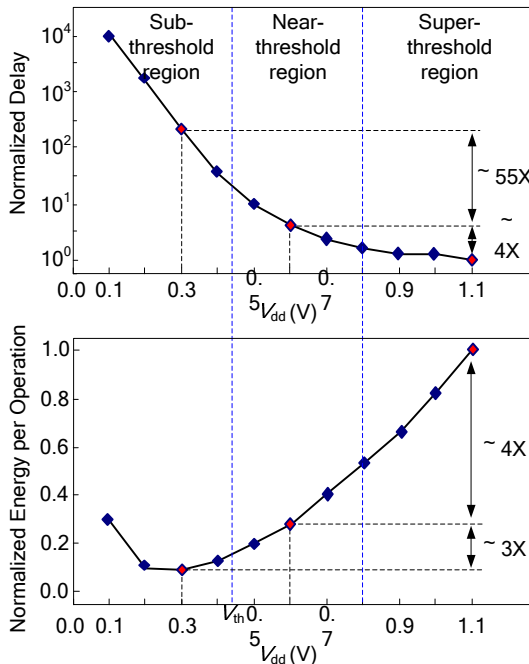


Figure 2. Energy and delay in different supply voltage operating regions.

According to the results, it can be found that the optimum energy point of the circuit is in the sub-threshold region. Energy typically reduces by 12X when  $V_{dd}$  is scaled from the nominal voltage to the sub-threshold regime, while delay rises about 200X.

When increasing the voltage from sub-threshold regime to near-threshold regime (500-700mV), the performance of the circuit increases about 55X than operating in the near-threshold regime with 3 times energy consumption. The operation frequency of the circuits in the near-threshold regime can reached about 300MHz-1.0GHz.

### A. Leakage Currents in Near-threshold Circuits

The leakage current of MOS devices in different state is investigated with voltage scaling. The behaviors of gate leakage current ( $I_{gate}$ ) and sub-threshold leakage current ( $I_{sub}$ ) of 45nm NMOS device are simulated using PTM BISM4 model at room temperature with supply voltages varies from 0.1 to 1.1V. The results of NMOS I-V characteristics are shown in Figure 3.

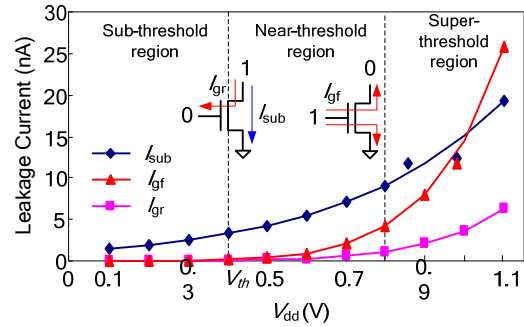


Figure 3. Leakage current of NMOS versus supply voltage.

The  $I_{gf}$  is about 33% larger than  $I_{sub}$  at nominal supply voltage (1.1V). However, with the supply voltage scaling, the gate leakage current decreases dramatically. In the near-threshold region (0.4-0.8V),  $I_{gf}$  reduced about 10-4173 times compared with that in the super-threshold region. The gate leakage current  $I_{gf}$  and  $I_{gr}$  are only 16.3% and 5.5% of  $I_{sub}$  when  $V_{dd}=0.6\text{V}$ . Hence,  $I_{sub}$  is the main component leakage current in MOS devices operation in the near-threshold region.

## III. GATE-LENGTH BIASING TECHNIQUES

### A. Gate-length Biasing Effect in NanoCMOS Devices

Leakage currents

In modern CMOS technology, as channel length becomes shorter,  $V_{th}$  shows a greater dependence on channel length, due to the short-channel effect (SCE) and drain induced barrier lowering (DIBL).  $V_{th}$  change due to SCE and DIBL is modeled [8]

$$\Delta V_{th}(SCE, DIBL) = -\theta_{th}(L_{eff}) \cdot [2(V_{bi} - \Phi_s) + V_{ds}] \quad (1)$$

where  $V_{bi}$ , known as the built-in voltage of the source/drain junctions,  $V_{ds}$  is the source/drain voltage. The short channel effect coefficient  $\theta_{th}(L_{eff})$  in (1) has a strong dependence on the channel length given by

$$\theta(L_{eff}) = \frac{0.5}{\cosh(L_{eff}/l_i) - 1} \quad (2)$$

$l_i$  is the characteristic length of devices.

According to (1) and (2), with increasing of the gate length, the threshold voltage increases, so that the leakage power decreases exponentially. Therefore, it is possible to slightly increase the gate length to take advantage of the exponential leakage reduction.

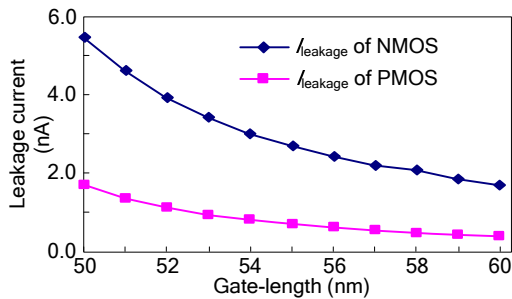


Figure 4. The variation of leakage of NMOS and PMOS devices with gate-length at a 45nm technology,  $V_{dd}=0.6V$ .

The variation of leakage with gate length ( $L_{Gate}$ ) is shown in Figure 4 at a 45nm CMOS process. The nominal gate length is 50nm, and the width of PMOS and NMOS transistors is 1000nm. It can be found that leakage current decreases exponentially with slightly increase of gate length. The leakage current of NMOS reduces by 51% and 69% at  $L_{Gate}=55nm$  and  $L_{Gate}=60nm$  compare with that of nominal length NMOS, respectively. And, the leakage current of PMOS reduces by 59% and 76%, respectively. Note that leakage current flattens out with gate-length beyond 55nm, making Gate length biasing less desirable in that range.

#### B. Cost-effective Gate Length Optimization Method

The key question in gate-length biasing methodology is the value of  $L_{Gate}$  for each transistor in the circuits. In this section, we propose a cost-effective gate length optimization method based on simulation by using a 12-stages inverter ring oscillator.

The variation of delay and leakage with gate-length of the inverter ring oscillator is shown in Figure 5 for a 45 nm CMOS process. It is obviously that with increasing of the gate length, the leakage power decreases exponentially and the delay increases linearly. Therefore, increasing gate lengths slightly can decrease leakage dissipation effectively, while circuit performance has a little penalty.

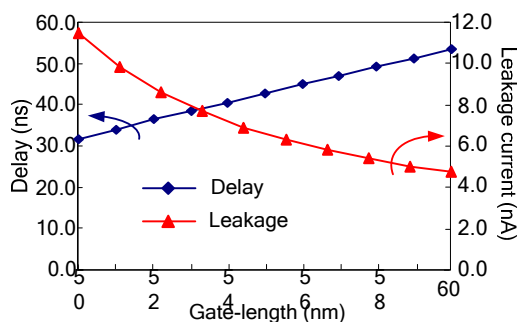


Figure 5. The leakage and delay of the inverter ring oscillator.

To determine the value of  $L_{Gate}$  for transistors, the cost-effective function is presented as follows

$$f_c(L_{Gate}) = \left| \frac{\Delta I_l}{I_{l0}} \right| - \Delta T_d / T_{d0}, \quad (3)$$

where  $I_{l0}$  and  $T_{d0}$  are the leakage current and delay of nominal  $L_{Gate}$  ring oscillator, respectively. The maximum

value of  $f_c(L_{Gate})$  means the best cost-effective, so the optimized  $L_{Gate}$  can be easily obtained. Figure 6 shows the  $f_c(L_{Gate})$  of the ring oscillator.

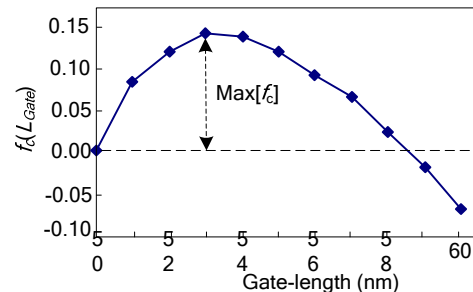


Figure 6.  $f_c(L_{Gate})$  with gate-length of the ring oscillator.

According to the Figure 6, it can be found that  $f_c(L_{Gate})$  has the maximum value when  $L_{Gate}=53nm$ . It provides one of the best tradeoffs between leakage power consumption and performance in low power applications.

#### IV. SIMULATION AND RESULTS

In this section, low-leakage power designs of the near-threshold basic gates is presented, which include basic logic gates such as NAND, NOR, XOR, and 1-bit full adders.

All the circuits are simulated with HSPICE at 45nm CMOS technology. The nominal gate length is 50nm, and the optimization length is 53nm. The supply voltage of the near-threshold circuits is 0.6V. In order to simulate the work environment of the basic logic gates, the testing platforms are shown in Figure 7. The delay and leakage currents of the circuits in the box are tested. In order to assure the fairness of the comparison, the two inverters are paralleled after all outputs to act as load capacitances, and the same input is given to these circuits.

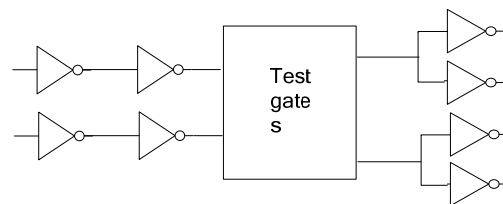


Figure 7. Test platform of basic logic gates.

#### A. Low-Leakage Basic Gates with Gate-Length Biasing

The basic gates such as inverter, NAND, NOR and XOR are important elements in digital circuits, since they are largely used. The basic logic gates are based on standard CMOS logic. HSPICE simulations are carried out for the basic gates.

The leakage current and delay of NAND2, NOR2 and XOR2 are shown in Table 1. The results show that the basic gates with the gate-length biasing technology have lower leakage than the one with the standard gate-length. The NAND2, NOR2 and XOR2 provide leakage reduction of

26.8%, 33.3% and 25.2% respectively. However, the delay of those gates is larger than the standard gate-length ones.

TABLE I. LEAKAGE CURRENT AND DELAY OF BASIC GATES

IN	Leakage Current(nA)					
	NAND2		NOR2		XOR2	
	50nm	53nm	50nm	53nm	50nm	53nm
00	0.45	0.41	1.22	0.86	2.72	1.74
01	1.27	0.89	0.66	0.37	3.00	1.98
10	0.92	0.69	0.43	0.26	2.79	1.82
11	0.65	0.41	0.10	0.11	2.43	1.52
$I_{av}$	0.82	0.60	0.60	0.40	2.73	1.77
$\Delta I\%$		-26.8		-33.3		-25.2
Delay(ps)						
$T_d(ps)$	63.0	75.3	67.7	79.0	160.1	193.5
$\Delta T_d\%$		19.5		16.7		20.9

**B. Low-Leakage Full Adders with Gate-Length Biasing**

The full adder is an important element in the digital datapath. Figure 8 shows the two commonly used full adder: mirror full adder (MFA) and transmission-gate full adder (TFA). The leakage and delay of the two adders are simulated using HSPICE.

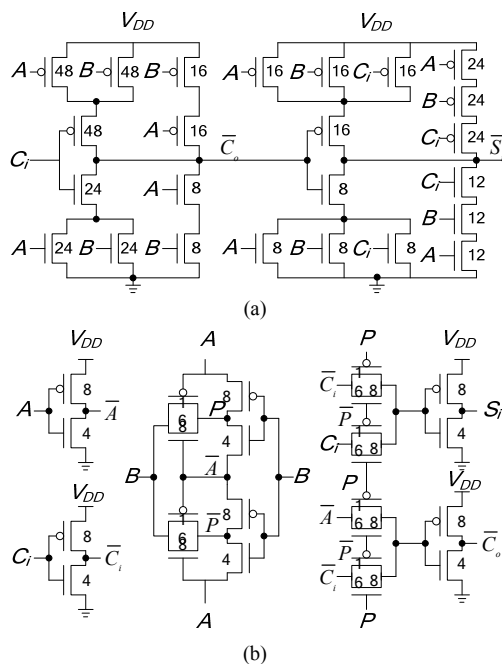


Figure 8. Two full adders, (a) mirror adder, (b) transmission-gate adder.

The device size of the two adders is shown in Figure 8, where  $\lambda=25\text{nm}$ . The simulation results are shown in Figure 9. In the Figure 9, MFA\_UN and TFA\_UN are the leakage current of the standard mirror full adder and transmit adder, respectively. MFA\_BIAS and TFA\_BIAS are the leakage current of the gate length biased mirror full adder and transmission-gate adder, respectively.

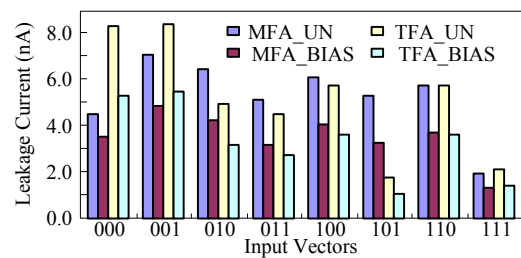


Figure 9. Leakage current of adders

Compared with standard adders, the leakage current of the biased MFA and TFA reduces 33.2% and 35.9%, respectively. While the delay of the biased mirror full adder and transmit adder increases 12.4% and 14.0%.

**V. CONCLUSION**

Leakage power is an important contributor of the total power dissipation in the modern CMOS circuits, even in the near-threshold logic circuits. In the paper, we present a leakage reduction method for near-threshold circuits using gate-length biasing technique. A cost-effective gate length optimization method is proposed to determine the gate length. The basic gates and two full adders with length biased are implemented and simulated using HSPICE at 45nm process. Simulation results show the gates with length biased reduced leakage current by 25.2%-35.9% comparison with standard gate length ones.

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