Optical Proximity Correction Using a New Hyper Error Estimation Method

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***Abstract*—In recent years, semiconductor manufacturing process has made great progress. To avoid lithography hotspots and enhance the yield of integrated circuits, we can use Model-based Optical Proximity Correction (MBOPC) to improve image fidelity and printability. However, the optical lithography simulation of MBOPC is a time-consuming calculation. In this paper, we propose an effective MBOPC to obtain a modified mask with high-resolution. The proposed OPC flow is divided into three steps: (1) *Pre-simulation* generates a set of modified value for each pattern, (2) *Grid-based Partition* can speed up MBOPC process and overcome alignment problem, and (3) a set of hotspot detection formulas detects the variation sub-area. The first and second steps will improve performance of lithography, and the third step will improve image fidelity. The experimental results of our procedure show that the average of edge placement error (EPE) within the marked area can be decreased from 259.76*um* to 7.24*um,* and bitmap error (BME) within the marked area can be decreased from 20.01% to 3.15%.**

Keywords- mask, optical simulation; OPC; model-based OPC

I. INTRODUCTION

Over the last few years, optical lithography processes improved from G-line (436nm), I-line (365nm), KrF (248nm) process to the current ArF (193nm) process technology. The feature size of IC has been smaller than the wavelength of the mainstream ArF 193nm lithography based on Moore's Law [7]. Therefore, consideration of the aspect of physical optics, it might make a severe impact on the IC manufacturing process regardless of any slight change [6][14], as shown in Figure 1(a) shows that mask has a hotspot area, and (b) is bridge image.

Figure 1. Bridged image may cause circuit short.

What has to be noticed is the process variation, which may incur latent process hotspots and yield loss [8]. Hence, there are some approaches applied to mitigate the effects of the lithographic process, which are also called resolution enhancement technology (RET). Those techniques, such as phase-shifted mask (PSM), e-beam proximity effect correction, off-axis illumination (OAI) [3] and various methods of optical proximity correction (OPC) as shown in Figure 2 [1][4][12]. In semiconductor manufacturing, OPC is a common way used in optical lithography to improve the imaging variation problem and improve layout mask quality [5].

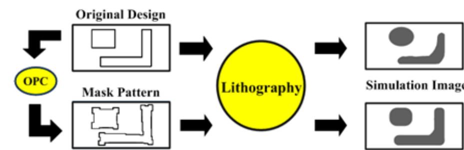

Figure 2. Conceptual approach to OPC.

The two main classifications of OPC are rule-based and model-based. Rule-based OPC is a simpler technique, which is to obtain the reliable geometry data of the pattern features, and then apply to the layout mask by looking up the bias table [10]. The model-based OPC (MBOPC) considers several process effects and optical parameters to simulate the layout pattern and apply a feedback system back and forth to end up with an optimal result. MBOPC is more complex and time-consuming. However, the reliability and accuracy of the results are significantly improved than those of Rule-based OPC.

In this work, we primary use the model-based OPC to complete the whole OPC flow, and adapt fast lithography simulation techniques from Cobb and Yu [4][12], and use it to reduce the computing time of convolution for the mask pattern simulation. Furthermore, we define a set of hotspot detection formulas to determine the *Hotspot_cost* value of each sub-area, and then use the *Hotspot_cost* value as the reference data for compensating mask pattern in our *MBOPC Feedback System*.

II. PROBLEM FORMULATION

The problem inputs are mask design (GDS file or CIF file) and lithography model [1]. The lithography model includes parameters of lithography process and manufacturability constraints. The lithography model is the sum of coherent system (SOCS) method as formula (1) and (2).

$$image_{sim}(x,y)=\frac{\sum_{k}^{N_k} weight_k\left|kernel_k(x,y)*mask(x,y)\right|^2}{\sum_{k}^{N_k} weight_k\left|kernel_k(x,y)*1\right|^2} \quad (1)$$

$$kernel_k(x,y)=\frac{\cos(\rho_k^2(x^2+y^2))}{\beta_k+\alpha_k\rho_k^2(x^2+y^2)}\exp\{-i2\pi(f_k x+g_k y)\rho_k\} \quad (2)$$

To develop an efficient and accurate OPC method to correct original mask design, we consider the following problem. Our objective is to modify the conventional MBOPC to overcome the time-consuming problem. Moreover, we propose an effective hotspot detection method

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to locate the critical area, and utilize the feedback system to correct critical area.

III. MBOPC METHODOLOGY

Our MBOPC flow is shown in Figure 3. There are three main steps, *Pre-simulation*, *Grid-based Partition* and *MBOPC Feedback System*. Note that, we will also introduce the *Hotspot Estimation* which is included in *MBOPC Feedback System*.

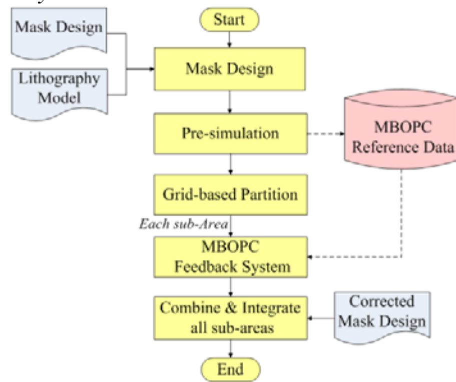

Figure 3. Overall flow.

A. Pre-simulation

Before the main process of MBOPC flow, we will execute a series of test pattern simulation, called *Pre-simulation*. Critical dimension provides useful information for lithography process [4][9]. Hence, we use *Pre-simulation* to get variations. In this step, we will analysis and record some variations by using several particular pattern features; we adopt some common patterns, such as the situations of Line-Bridging [11], Corner Rounding, the smallest printable width also called Line-End width and L-Shape Jog (Inside Corner and Outside Corner), as shown in Figure 4.

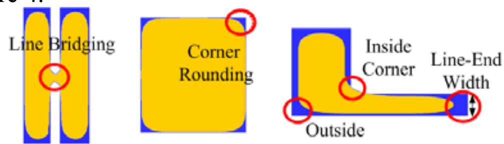

Figure 4. Some major pattern features and variations.

B. Grid-based partition

Considering the chip size and the complexity of the input mask design, we will partition the whole mask layout pattern into proper sub-area with the same size before MBOPC procedure, as shown in Figure 5.

The formulation is as follow, first we define the input pattern set $P = \{P_1, P_2, \ldots, P_i\}$, and each pattern is assigned to partitioned grid *sub-area*(m,k) which overlaps with that pattern.

$$1 \leq m \leq \left\lceil \frac{chip\ width}{maximum\ spacing} \right\rceil = X, 1 \leq k \leq \left\lceil \frac{chip\ height}{maximum\ spacing} \right\rceil = Y \quad (3)$$

X and *Y* denote the maximum index of the sub-area set on x-axis and y-axis separately, as formula (3). The *chip width* and *chip height* represent the full chip width and height. The *maximum space* is the maximum chip height represent the maximum space which may bring up optical proximity effects between two neighboring patterns, in this contest, the maximum space can refer to the kernel ambit; *m*, *k*, *X* and $Y \in N$, $N = \{0,1,2,3,\ldots\}$.

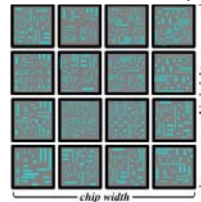

Figure 5. Dividing the whole layout into several sub-area.

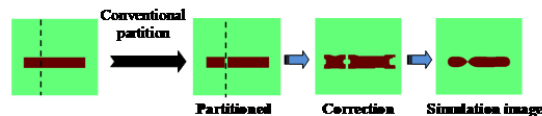

Figure 6. Alignment problem.

We observe that the partition method of conventional research may cause the alignment problem [13][15] as shown in Figure 6. Therefore, we must analyze one partitioned grid with its neighboring grids. Our *Grid-based partition* method can reduce the amount of pattern numbers for pattern analysis in each sub-area, and avoid the unnecessary analyzing. For example, we partitioned the entire domain in Figure 7(a) into sub-area with equal spacing in x and y direction as shown in Figure 7(c). In order to minimize the interacting region, we set the spacing of each grid to maximum interacting distance; maximum spacing is the kernel ambit being mentioned in lithography model. In Figure 7(c) shows the results through the *Grid-based Partition* approach considering the pattern integrity, pattern 1 is assigned to *sub-area*(1,0) , pattern 2 is assigned to *sub-area*(1,0) and *sub-area*(1,1) , pattern 3 is assigned to *sub-area*(0,0) and *sub-area*(0,1), and pattern 4 is assigned to *sub-area*(0,1). For instance, *sub-area*(1,0) stores the complete information of pattern 1 and 2.

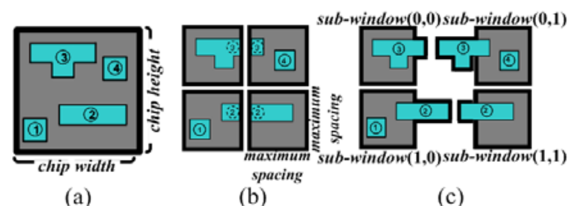

Figure 7. (a)Layout domain. (b)Conventional Partition. (c)Grid-based Partition.

The *Grid-based partition* method can decrease the memory usage, and speed up the performance. Furthermore, we can overcome the alignment problem and prevent the yield loss from conventional partition techniques.

C. Hotspot estimation

In semiconductor manufacturing process, the hotspots usually cause defects of chip. Such that, we develop a set of estimation method called *Hotspot Estimation*. Our estimation incorporates two effective measuring methods, the edge

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placement error and the bitmap error as the basis for MBOPC.

*1) Edge placement error:*After the step of setting control points, the edge of every polygon will be fragmented into several segments. And the edge placement error is the absolute summation of the difference between the printed edge position and the original pattern edge position from every control point, as shown in Figure 8 shows that EPE value is summation of the A, B, C and D.

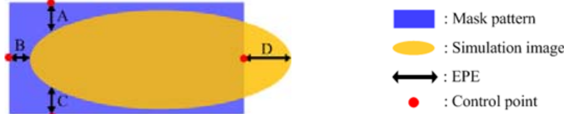

Figure 8. Edge placement error.

2) Bitmap error: The bitmap error is used to measure the variation between the original design pattern and the simulation image. BME is the average absolute summation of the difference of every pixel withins each sub-area.

In our MBOPC procedure, we use a new cost function to determine the degree of the variation problem within each sub-area, as shown in Figure 9.The *Hotspot_cost* function of our system can be defined as follows.

$$\begin{aligned} & Hotspot_cost \\ &= \alpha \times BME + \beta \times \frac{EPE}{\#TotalCPs} \\ &+ \gamma \times \frac{\#BridgedCPs}{\#TotalCPs} + \omega \times \frac{\#BrokenCPs}{\#TotalCPs} \end{aligned} \quad (4)$$

Here, α,β,γ and ω are the user-defined parameters to control the weight between *EPE* and *BME*. *#TotalCPs* is the total control point number on every polygon within each sub-area. *#BridgedCPs* is counting bridged control points when contour images overlap or intersect. *#BrokenCPs* is counting break control points when a contour image breaks or disappears.

Figure 9. To determine the bridged or break within each sub-area.

As mention before we combine EPE and BME as our *Hotspot_cost*. The reason is that EPE can help our MBOPC to precisely estimate the variation; moreover, we also use BME to obtain the overall error within each sub-area before and after MBOPC. Therefore, we use the *Hotspot_cost* function (4) to detect critical area and correct.

D. MBOPC feedback system

Recalling the previously mentioned overall flow (see Figure 2), here we will introduce how the *MBOPC Feedback System* works, as shown in Figure 10.

Input is the sub-area which be partitioned from the original mask design. First, the procedure would execute Fast Simulation for input area to obtain *Hotspot_cost* which be mentioned in Section 3.3. Then we use *Hotspot_cost* to estimate the MBOPC results after each mask correction; if the current solution meets our defined tolerance, the corrected mask pattern of the input area will be accepted and stored. In addition, if the iteration of mask correction is more than our defined limit, the procedure will stop and pick out the best solution from *Solution Center*.

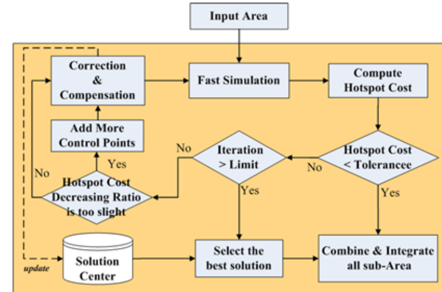

Figure 10. MBOPC Feedback System.

In fact, before *Fast Simulation* our procedure has already added a small amount of control points on the polygons within input area. Therefore, we can correct and compensate the polygons by shifting these movable segments inwards or outwards. Furthermore, we add a step in our *MBOPC Feedback System* to enhance the mask resolution. This technique will add more control points on the edge of every polygon according to the degree of the variation problem. If the *Hotspot_cost* decreasing ratio is too slight and *Hotspot_cost* does not meet our tolerance after several mask corrections, which means the variation problem is still exist but the fragmented segments are not precise enough, our procedure will fragment the current segments into more precise segments to achieve a better solution. In this way, we can save the execution time of our MBOPC procedure by refining the correction solution for the area with high variation problems.

IV. EXPERIMENTAL RESULTS

We have implemented the program in C/C++, complied with GCC 4.1.1, and all the experiments are performed on a Windows XP operating system. We use a layoutEditor tool library [2] as our test case. The cases shown in TABEL II include size and layers. We extract one metal layer to illustrate our procedure. Furthermore, our simulation is according to 2011 CAD Contest Problem B1 [1], TABLE I is lithography model includes parameters of lithography process and manufacturability constraints. SOCS_KER_AMBIT is effective proximity range of SOCS kernels. The model has four kernels (Formula 2), parameters is SOCS_KER_PARs. MASK_MIN_LENGTH is minimum length of mask segment. To shift edge must be multiple of MASK_MIN_SHIFTING. Mask area must be larger than MASK_MIN_AREA.

TABEL III shows values of BME and EPE in our *MBOPC Feedback System*. Before MBOPC column is the original value of BME (avg_EPE). After MBOPC column is the correction value of BME (avg_EPE). Improvement column is the difference between before and after MBOPC. As shown in TABEL III, BME and EPE are decreased significantly, because our Hotspot Estimation can locate the

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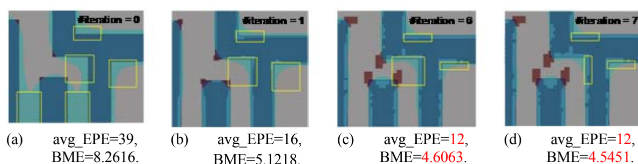
critical area effectively, and we utilize the *MBOPC Feedback System* to correct critical area.

TABLE I. LITHOGRAPHY MODEL.

SOCS_KER_AMBIT (*nm*)	512				
SOCS_KER_PARs	*f*	*g*	*ρ*	*α*	*β*
	+0.6	-0.6	0.01	2.1	0.9
	-0.6	+0.6	0.01	2.1	0.9
	-0.6	-0.6	0.01	2.1	0.9
	+0.6	+0.6	0.01	2.1	0.9
MASK_MIN_LENGTH (*nm*)	10				
MASK_MIN_SHIFTING (*nm*)	1				
MASK_MIN_AREA (nm^2)	400				
PHOTO_RESIST_THRESHOLD	0.28				

TABLE II. CASE TYPE.

Circuit	Size (*um*)	Layers
Case1 (MUX2_X1)	3.0×3.2	5
Case2 (CLKGATE_X4)	4.9×3.2	4
Case3 (DFFS_X2)	3.8×1.6	5
Case4 (SDFFR_X2)	5.1×1.6	5



(a) avg_EPE=39, BME=8.2616. (b) avg_EPE=16, BME=5.1218. (c) avg_EPE=12, BME=4.6063. (d) avg_EPE=12, BME=4.5451.

Figure 11: BME and EPE in our MBOPC Feedback System.

Furthermore, we also experiment DFFS_X2 to verify the effectiveness of BME and EPE in our *MBOPC Feedback System*. As shown in Figure 11, the yellow rectangle area is bridged (or broken) control points. Obviously, the value of avg_EPE is the same during the #iteration 6 and 7(Figure 11.(c) and (d)). As our experience, the MBOPC will be stopped and produce worse results (Figure 11.(c)) if we only took the avg_EPE as our *Hotspot_cost* function. Therefore, we proposed the *Hotspot_cost* (4), then our MBOPC can take the BME into consideration and get better results (Figure 11.(d)).

V. CONCLUSION

We introduce an effective *MBOPC Feedback System* for correcting mask patterns. The *MBOPC Feedback System* uses our defined hotspot estimation to determine the *Hotspot_cost* value within each sub-area. When the *Hotspot_cost* value can't be improved we can enhance the mask resolution by the step of adding more control points. The experimental results show that we can correct the mask design of the test case, the avg_EPE within the marked area can be decreased from 259.76*um* to 7.24*um,* and BME within the marked area can be decreased from 20.01% to 3.15%.

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REFERENCES

[1] http://cad_contest.cs.nctu.edu.tw/cad11/Problem/99/CAD2011_ProblemB1_update20110221.pdf

[2] http://www.layouteditor.net/

[3] K. Agarwal, "Frequency Domain Decomposition of Layouts for Double Dipole Lithography," in Proceedings of ACM/IEEE DAC, pp. 404–407, June 2010.

[4] N.B. Cobb, "Fast Optical and Process Proximity Correction Algorithms for Integrated Circuit Manufacturing," PhD Dissertation. Dept. Electrical Engineering and Computer Science, University of California at Berkeley, 1998.

[5] K. Cao and J. Hu, "ASIC design flow considering lithography-induced effects," in Proceedings of Circuits Devices & Systems IET, pp.23-29, February 2008.

[6] L.R. Harriott, "Limits of lithography," in Proceedings of IEEE, pp.366–374, March 2002.

[7] T. Jhaveri, V.Rovner, L. Liebmann, L. Pileggi, A.J. Strojwas and J.D. Hibbeler, "Co-Optimization of Circuits, Layout and Lithography for Predictive Technology Scaling Beyond Gratings," in Proceedings of IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 29, pp.509–527, April 2010.

[8] R. Raina, "What is DFM & DFY and Why Should I Care ?" in Proceedings of ITC, pp.1-9, October 2006.

[9] J.S. Park, C.H. Park, S.U. Rhie, Y.H. Kim, M.H. Yoo, J.T. Kong, H.W. Kim and S.I. Yoo, "An Efficient Rule-based OPC Approach Using a DRC Tool for 0.18μm ASIC," in Proceedings of ISQED, pp. 81–85, March 2000.

[10] R. Shi, Y. Cai, X. Hong, W. Wu and C.Yang, "The Selection and Creation of the Rules in Rules-Based Optical Proximity Correction," in Proceedings of International ASIC Conf, pp. 50–53, October 2001.

[11] M.D. Stewart, G.M. Schmid, S.V. Postnikov and C.G. Willson, "Mechanistic Understanding of Line End Shortening," in Proceedings of SPIE, vol. 4345, pp.10-18, August 2001.

[12] P. Yu, S.X. Shi, D.Zi Pan, "Process variation aware OPC with variational lithography modeling, " in Proceedings of ACM/IEEE DAC , pp.785-790, July 2006.

[13] S.M. Yu and Y. Li, "A Pattern-Based Domain Partition Approach to Parallel Optical Proximity Correction in VLSI Designs," in Proceedings of IPDPS, pp.4-8, April 2005.

[14] Y.S. Tong, S.J. Chen, "An Automatic Optical Simulation-Based Lithography Hotspot Fix Flow for Post-Route Optimization," in Proceedings of TCAD, p.p. 671-684, May 2010.

[15] Y. Kumar and P. Gupta, " Reducing EPL Alignment Errors for Large VLSI Layouts," in Proceedings of ISQED, p.p. 233-238, March 2007.

TABLE III. EPE AND BME RESULTS.

ircuit	BME			avg_EPE		
	Before MBOPC	After MBOPC	Improvement	Before MBOPC	After MBOPC	Improvement
Case1	45.55	30.30	33.47%	215	81	62.33%
Case2	103.64	70.49	31.98%	348	94	72.99%
Case3	19.53	13.79	29.39%	126	70	44.44%
Case4	77.69	51.91	33.19%	336	91	72.92%

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