Design of a High Performance 5.2 GHz Low Phase Noise Voltage Controlled Oscillator Using 90nm CMOS Technology

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***Abstract*—In this paper, a novel Figure of Merit (FOM), low phase noise, LC-tank voltage-controlled oscillator (VCO) is presented. The work presents a fully integrated 5.2 GHz VCO designed in a 90nm CMOS process. The proposed VCO features a worst-case phase noise of -130.10dBc/Hz and -133.00 dBc/Hz at 600 kHz and 1 MHz frequency offset from 5.2GHz carrier is achieved. An optimization technique is used to design the excellent FOM. The FOM is -206.02dBc/Hz. It features a supply voltage of 2.7 V, with a core of only 0.5 mA.**

***Keywords*-design method; figure of merit; low phase noise, CMOS technology.**

I. INTRODUCTION

The recent exponential growth in wireless communication has increased the demand for more available channels in mobile communication applications. In turn, this demand has imposed more stringent requirements on the phase noise of the VCO. The integrated inductance–capacitance (LC) VCO is one of the most important components in today's communication systems. They are among the key building blocks of RF systems, and are used for carrier frequency synthesis to up-convert and down-convert signals. Their output frequency is stabilized or controlled with a Resonator. It seems that every wireless instrument in use today has some sort of VCO inside it. In particular, every cell phone that generates radio frequency (RF) waves contains at least one VCO. Despite the continuous development and wide improvements in CMOS VCOs, it is now generally recognized that they still remain the most critical part of RF transceivers.

The phase noise of the VCO is used to describe phase fluctuations due to the random frequency fluctuations of a signal. Phase noise can be caused by a number of conditions, but is mostly affected by VCO frequency stability. It is one of the most important parameters for the quality and performance of information transfer, in turn affecting the reliability purposes in data communication. Consequently, achieving low phase noise and low power consumption specifications, VCOs are a major design challenge and thus have received a lot of attention in recent years. Recently many state-of-the-art integrated LC CMOS VCOs have been implemented in 0.18µm CMOS technology. Designers have tried to improve the phase noise performance of LC-VCO and new phase noise theories have been proposed [1]-[5]. Even for these optimized VCOs, the excellent phase noise performance obtained is still limited by the quality factor of the integrated inductors. To achieve the low-phase-noise specifications, an integrated LC-VCO seems to be the best choice. The design depends specifically on the integration of a high-quality LC tank.

This paper is organized as follows. Section II considers the circuit design method used to minimize the phase noise. Section III presents the implementation and measured results, followed by the conclusion in Section IV.

II. VCO DESIGN AND IMPLEMENTATION

The schematic of our LC-VCO design is shown in Fig. 1. The implemented VCO uses a complementary cross-coupled topology. The performance was implemented in a standard 0.09μm CMOS process. This schematic has been chosen because it can have large signal swings as well as generate symmetric signals. Oscillation frequency is determined by the inductance and capacitance values in the LC tank.

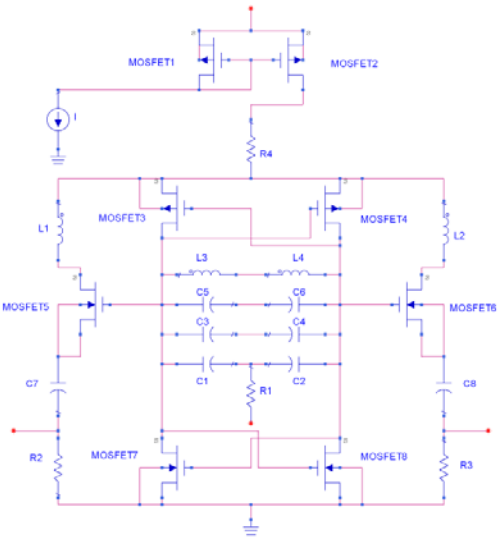

Fig. 1. Complementary cross-coupled VCO.

VCOs are generally designed for minimum phase noise under constraints of D.C. power dissipation, tuning range, output voltage swing and die area. The chosen topology of this VCO was selected as the loss of the LC tank will be compensated by the cross-coupled NMOS and PMOS

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differential pairs, which provide a negative resistance and generate symmetric signals [6]. The oscillation frequency was determined by the inductance and capacitance values in the LC tank. Inductance and capacitance of the LC tank was determined and the targeted centre frequency was chosen to be 5.2 GHz.

The double cross-connect NMOS (MOSFET7-MOSFET8) and PMOS (MOSFET3-MOSFET4) differential pairs provide the negative resistance to cancel losses in the LC resonator. Fundamentally, phase noise is limited by the Q factor of an LC tank although the VCO circuit is well designed and fully optimized. For further phase noise reduction, higher Q is inevitable. The VCO circuit should have lower transconductance for minimum phase noise as Q increases [7]. Therefore, the VCO circuit also has to be optimized as Q changes in order to fully utilize the high Q factors of an LC tank. The CMOS transistors must be biased and laid out such that the required gm is obtained to overcome all losses including those of the tank and the transistors. The respective trans-conductance of each pair was kept the same which was equal to $g_m/2$. Hence, the total negative trans-conductance became $-g_m$. As a result, less current was used and the loss of tank circuit was compensated; as a consequence, this led to lower power consumption.

The primary challenge in designing VCOs is minimizing phase noise while maintaining smallest power consumption, which can be achieved by improving the quality of the resonator. In order to reduce the phase noise of this work, some techniques and several steps were taken into consideration in order to achieve the best phase noise. Firstly, the tail transistors of the current mirror design were implemented using PMOS (MOSFET1-MOSFET2) components which offer a high precision current source and in terms of noise it is less than the NMOS mirror current circuit. Secondly, it is well known that phase noise decreases inversely proportional to the square of the quality factor (Q) in an LC tank [7]. Therefore, the capacitors of this design not only consisted of the variable capacitor to tune the oscillator, but also included fixed capacitances, the load and the active elements. Thirdly, transistor sizing was used to control the VCO current. In addition, the areas of the cross-coupled pair were kept slightly high to reduce 1/f noise. Fourthly, the inductors turned out to be near optimum for the oscillator design, as will be seen later. Relatively small L, high Q inductor values are the key to a good, low-power and low-noise oscillator. Finally, keeping the gm of the NMOS and PMOS at the same value helped to reduce the up-conversion of phase noise. The VCO outputs are buffered using buffer stages NMOS (MOSFET5-MOSFET6) to isolate the LC tank.

High density 90 nm technology has been suggested and implemented in this design for a generic, low voltage high performance application. It shows superior performance and reliability compared for example to similar 0.35µm CMOS structures; using this technology the circuit can be fabricated with standby power that is only 15% of other technologies.

The total capacitor of this design is approximately 4.68pF. The inductor turned out to be near optimum which is around 0.2nH for the oscillator design, with relatively small L and high Q inductor values, which are the key to a good, low-power and low-noise oscillator.

The physical dimensions *W/L* of the MOSFETs are maintained to be 2.5µm/0.09nm for optimum phase noise. The measured results demonstrate that the topology in this research is useful for achieving a lower phase noise. It can be shown that the oscillation frequency of an ideal tank and MOSFETs is given by:

$$w_o = \frac{1}{\sqrt[2]{LC}}\sqrt{1-\frac{R^2 C}{L}} \quad (1)$$

For oscillation to occur, the g_m of each MOSFET must be:

$$g_m \geq \frac{RC}{L} \quad (2)$$

Taking into consideration all the parasitic capacitance of the VCO MOSFETs, the frequency of oscillation can be derived as:

$$w_0 = \frac{1}{\sqrt[2]{L(C+C_{gs}+4C_{gd_0})}}\sqrt[2]{1-\frac{R^2(C+C_{gs}+4C_{gd_0})}{L}} \quad (3)$$

From this equation it can be clearly seen that the transistor capacitance, C, requires a decrease in C value compared to the ideal case for a given resonant frequency [7]. Real-world sources have an unwanted amplitude or phase of the signal. The start-up gm condition also changes such that the absolute minimum gm required for oscillation becomes:

$$g_m \geq \frac{1}{d_s} + \frac{R(C+C_{gs}+4C_{gd_0})}{L} \quad (4)$$

This equation states the importance of MOSFET size and the result is that the bigger it is the higher the gm must be to achieve oscillation.

A perfect VCO would be able to produce a pure signal. The following noise-free signal is represented in equation (5):

$$v(t) = A\cos(2\pi f_0 t) \quad (5)$$

Real-world sources have unwanted amplitude or phase of the signal [8]. These phase modulated components, known as phase noise, are added to this signal by adding a random variable (probability) process represented by φ to the signal as indicated in equation (6):

$$v(t) = A\cos(2\pi f_0 t + \varphi(t)) \quad (6)$$

To model the measured phase noise more accurately, Leeson's equation is used in which an expression describes an oscillator's phase noise spectrum for single-sideband (SSB) phase noise in dBc/Hz. L(fm) defines the ratio of power in a 1 Hz bandwidth away from the carrier to the carrier power, and is usually the important measure of noise around communications signals. This is SSB power which can be caused by a rise or fall in the amplitude or phase of the source, as well as additive broadband noise.

The phase noise of an LC-VCO is described in equation (7) as [9]:

$$L(f_m) = 10\log\left[\frac{1}{2}\left(\left(\frac{f_0}{2Q1f_m}\right)^2+1\right)\left(\frac{f_c}{f_m}+1\right)\left(\frac{FKT}{p_s}\right)\right] \quad (7)$$

where f_o is the output frequency, Q_l is the loaded Q, f_m is the offset from the output frequency, f_c is the 1/*f* corner frequency, *F* is the noise factor of the amplifier, *k* is Boltzmann's constant, *T* is absolute temperature in Kelvins, and P_s is the oscillator output power. For a CMOS oscillator, the noise factor, *F*, can be expressed as:

$$F = 1 + \frac{K_1\gamma I_{bias}R}{V} + K_2\gamma g_{bias}R \quad (8)$$

where K_1, K_2 are constant, γ is a FET noise factor, g_{bias} refers to the current source trans-conductance, R is the tank resistance, and V is the output voltage. The phase noise of the oscillator could be reduced by increasing the amplitude of the output signal from Leeson.

The power consumption of this VCO is inversely proportional to its phase noise level [7]. If the oscillation amplitude for a given voltage supply is wider, the VCO is more efficient. It is noticed that as the Q factor of the tank increases, phase noise decreases.

In the CMOS process, transistor noise is generally high and causes serious degradation of VCO phase noise performance. However, the noise of PMOS is usually lower than NMOS by one order of magnitude [7]. Moreover, the measured minimum noise figure of NMOS and PMOS transistors under exact bias level also shows clearly the noise of PMOS is lower than that of NMOS.

III. SIMULATION RESULTS

The implemented VCO was simulated using the Advanced Design System (ADS) produced by Agilent Technologies Inc**.** The circuit generates stable periodic signals with a harmonic index as shown in Fig. 2, and outputs as shown in Fig. 3 and Fig. 4 respectively.

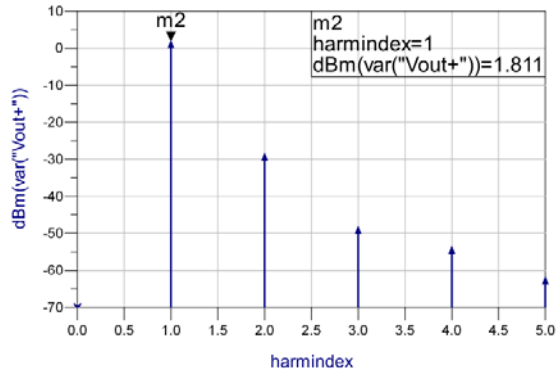

Fig. 2. Harmonic index of the VCO.

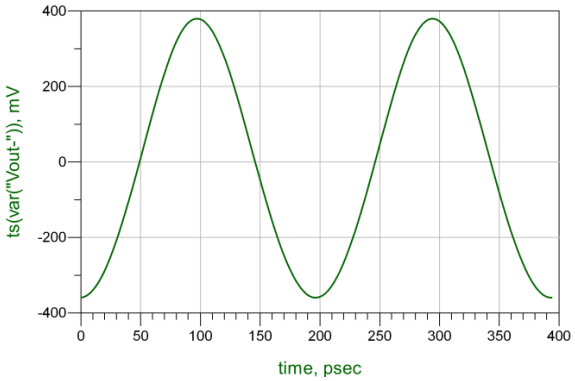

Fig. 3. V_{o+} output signal of the VCO.

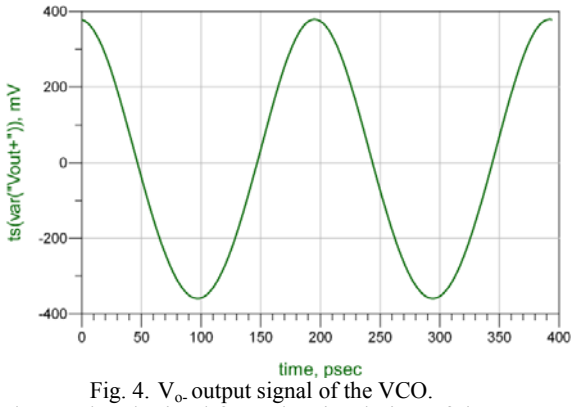

Fig. 4. V_{o-} output signal of the VCO.

The results obtained from the simulation of the LC- VCO design show that the phase noise have been drastically reduced.

A brief description of the performance summary is illustrated in Table I.

Table I. 5.2-GHz VCO Measured Performances

Supply Voltage (V)	2.7
Power Consumption (mW)	1.35
Tuning Range (GHz)	4.62-5.81
Tuning Voltage (V)	0-1.8
Resonance frequency, f_0 (GHz)	5.2
Phase Noise (dBc/Hz) at 5.2GHz	-130.1@600kHz offset.

The phase noise improves as the varactor gain decreases. Therefore, the worst phase noise is recorded as shown in Fig. 5.

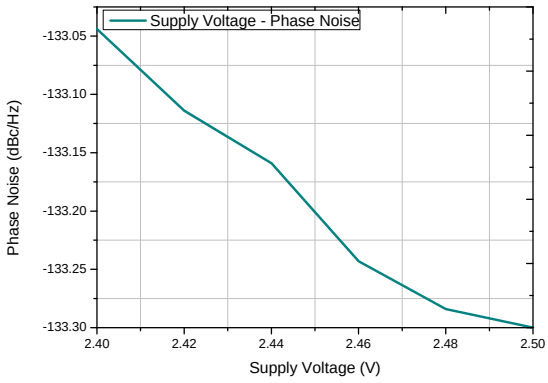

Fig. 5. VCO phase noise at 1 MHz offset frequency versus supply voltage.

The phase noise is automatically decreased while the power consumption is reduced. Thus, there is a trade-off between the power consumption and phase noise [7]. The phase noise can be achieved as shown in Fig. 6.

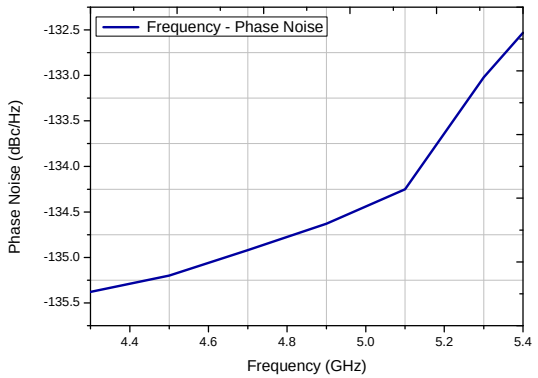

Fig. 6. VCO phase noise at 1 MHz offset frequency versus frequency.

The phase noise of -130.10 dBc/Hz and -133.00 dBc/Hz at 600 kHz and 1 MHz frequency offset are obtained at 5.2 GHz frequency as shown in Figs. 7 and 8 respectively.

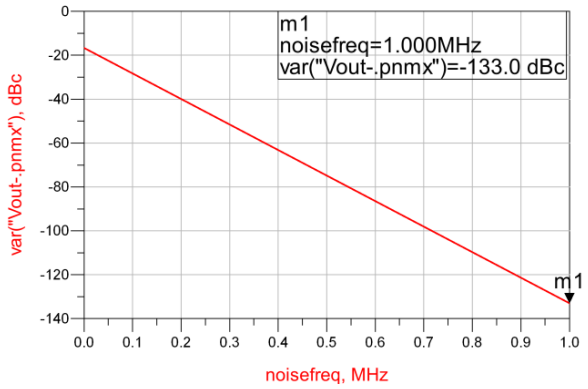

Fig. 7. Simulated phase noise at 1 MHz offset.

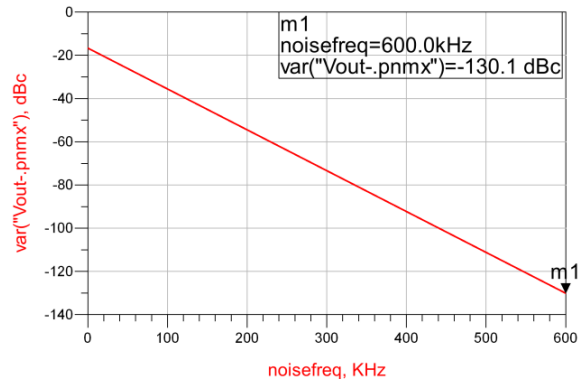

Fig. 8. Simulated phase noise at 600 kHz offset.

To compare the performance of previously published oscillators, and FOM, the one we have used was adopted by Ham and Hajimiri [10], and it normalizes the measured phase noise with respect to center frequency and power consumption. It is defined by equation (9):

$$FOM = L\{\Delta f\} - 20\log\left\{\frac{f_0}{\Delta f}\right\} + 10\log\left\{\frac{Pd}{1mW}\right\} \quad (9)$$

where Δf is the offset frequency, f_0 is the oscillating frequency, $L\{\Delta f\}$ is the measured phase noise at the offset frequency, and P_d (W) is the power dissipation of the VCO.

A brief description of the performance summary and comparison with published work has been mentioned in Table II, and shows that the design of the proposed VCO proved to be state of the art. The phase noise is considerably very good where the FOM is found to be excellent.

Table II. Summary of Measurement Results and Previously Reported VCOs, using CMOS

Process	Freq (GHz)	P/mW	PN (dBc/Hz)	Offset (MHz)	FOM (dBc/Hz)	Ref.
0.09μmCMOS	5.63	14.0	-108.50	1.0	-172.00	[11]
0.18μmCMOS	5.20	9.70	-113.70	1.0	-180.00	[12]
0.18μmCMOS	5.00	1.10	-117.70	1.0	-191.80	[13]
0.18μmCMOS	5.80	10.8	-117.00	1.0	-184.00	[14]
0.18μmCMOS	2.50	9.72	-128.70	1.0	-189.40	[15]
0.09μmCMOS	5.20	1.35	-133.00	1.0	-206.02	This Work

IV. Conclusions

We demonstrated a 5.2 GHz low-phase-noise and low-power LC-VCO based on cross-coupled topology using a 90nm CMOS technology. The feasibility of a high-performance, high-frequency VCO is demonstrated. The phase noise of the oscillator was optimized and the measured worst-case phase noise is -130.10 dBc/Hz and -133.00 dBc/Hz at 600 kHz and 1 MHz frequency offset, respectively. As a result, this CMOS VCO achieves the best FOM of -206.02 dB. The VCO shows approximately 22.9% tuning range and consumes 1.35mW from a 2.7 V power supply.

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