Development of waveform digitizing system for neutron detector

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***Abstract*—The neutron detector of HIRFL (Heavy Ion Research Facility at Lanzhou) has been designed for in-beam nuclear experiments, capable of measuring neutron energy and discriminating neutrons from gamma-rays. The read-out electronics, receiving charge signals from photomultipliers of the neutron detector, should be capable of acquiring data of three things including quantity of electric charge, time-to-flight and pulse fall time. For satisfying the physical requirements of high precision, high integration density and minimum cost, we have developed a waveform digitizing system that acquires all the required data in single read-out process. The waveform digitizing system is based on high-speed switched capacitor array (SCA) chip named DRS4 that allows sample an interested region of analog signal up to a rate of 5 GSPS. A 14-bit pipeline ADC and a FPGA are employed to digitize the charges stored in SCAs and deliver the waveform data to the host computer via PCI bus. The software completes fitting the waveform and calculates the required data. In this paper the detail of the electronics and algorithms of the waveform digitizing system is presented.**

Keywords: neutron detector, waveform digitization, switched capacitor array, analog-digital conversion

I. INTRODUCTION

The neutron detector of HIRFL[1] (Heavy Ion Research Facility at Lanzhou) has been designed for in-beam nuclear experiments. As is shown in Fig. 1, the heavy-ion beam collisions with the target generate neutrons and gamma-rays that are absorbed by liquid scintillators and photomultipliers (PMTs). The charge signals from PMTs are delivered to the data acquisition (DAQ) system. The energy of neutrons should be measured and the neutrons should be discriminated from the gamma-rays. To measure the neutron energy, the quantity of the charge signal that is proportional to the energy should be measured. To discriminate the neutrons from the gamma-rays, time-to-flight (TOF) and pulse fall time should be measured. The PMT charge signals are fast signals with some features: rise time of less than 5 ns, TOF of less than 300 ns and fall time of less than 300 ns. Traditionally, we use charge integrating circuit and analog-to-digital converter (ADC) to measure the charge quantity, and use time-to-digital converters (TDC) and threshold discriminating circuits to measure the TOF and fall time. However, employment of three readout electronics brings high cost and low integration. An alternative to the traditional readout electronics is the waveform digitization that can acquire all required information by analyzing the acquired digital waveform. The traditional waveform digitization based on flash-ADCs is not able to meet the requirement of high speed and high precision[2-3]. So we developed the DAQ system based on switched capacitor array (SCA) named DRS4[4-6] that is able to achieve the sampling speed of 5 GSPS without degrading the analog to digital conversion precision. The electronics design of the waveform digitizing system is described in detail below.

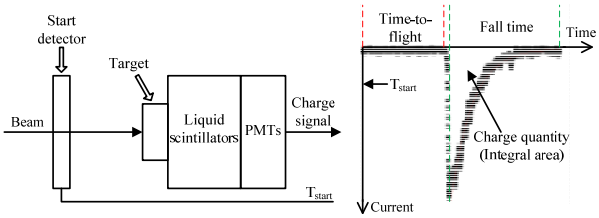

Figure 1. Neutron detector architecture and charge signal from PMT.

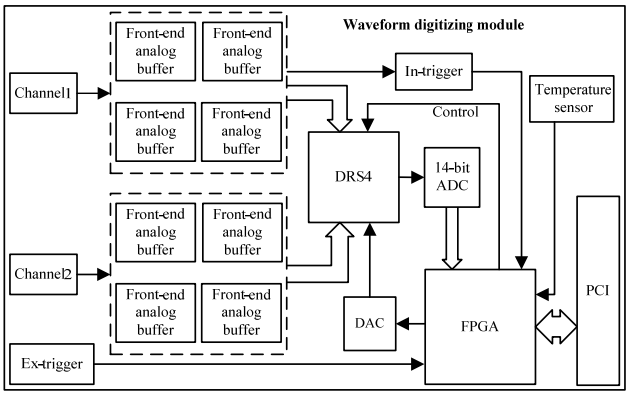

Figure 2. Architecture of waveform digitizing module.

II. THE IMPLEMENTATION OF WAVEFORM DIGITIZING SYSTEM

The waveform digitizing system is implemented in a 3U PCI module shown in Fig. 2. Receiving the external trigger from the start detector, the input analog signal from PMT is sampled and stored in capacitor arrays of DRS4 at sampling speed of 5 GSPS. The voltage values of charging capacitor arrays are then read out one by one for digitization. We usea 14-bit pipeline ADC (AD9245) that digitizes the output

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signals of DRS4 at a speed of 33 MSPS. A FPGA (EP1C12F324) is employed to receive the ADC outputs, control the digitizing system and communicating to the host computer via PCI bus. A temperature sensor and a DAC (LTC2600) are used to calibrate the working voltages of the front-end buffers and the DRS4.

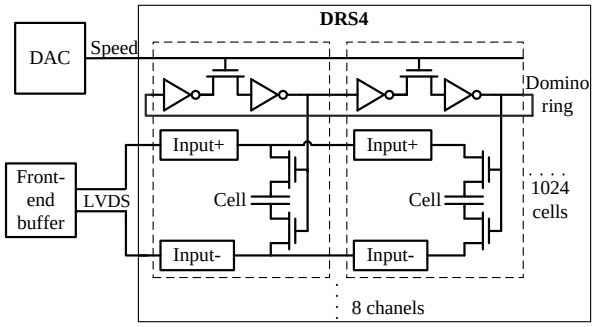

Figure 3. Simplified analog sampling circuit of DRS4.

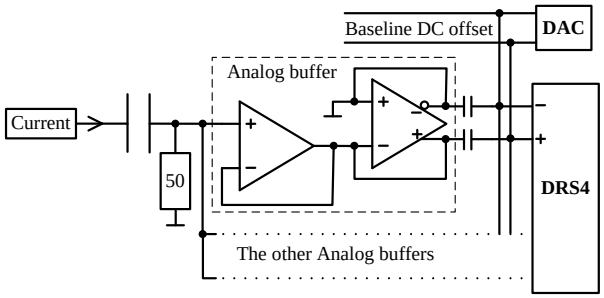

Figure 4. The front-end analog circuit.

A. DRS4 Sampling Circuit

DRS4 is a high speed SCA based on Domino Ring Sampling technology, developed at Paul Scherrer Institute. It is capable of sampling 8 differential input channels at sampling speed of 5 GSPS and storing the analog signals in 1024 sampling cells of each channel. Fig. 3 shows the DRS4 analog sampling circuit composed of the on-chip inverter chain (domino ring) and the analog sampling cells (on-chip capacitor arrays). Receiving the external trigger from the start detector, the domino signal propagates along the domino ring to open the switches of the sampling capacitors in square. The sampling speed is controlled by NMOS transistors between the inverters of each delay tap. We adjust the sampling speed to 5 GPSP via adjusting the transistor voltage supplied by a DAC to a proper value. The mechanism is that the transistor resistor and the inverter parasitic capacitance form an RC circuit, which generates a propagating delay of the domino ring. So the sampling speed is controlled by the transistor voltage which decides the transistor resistor. Because the required sampling time composed of TOF, rise time and fall time is up to 600 ns, every 4 channels of DRS4 are cascaded to achieve a sampling depth of 4096 cells so that the single sampling time can achieve 800 ns at the sampling speed of 5 GSPS. The cascaded 4 channels are switched in square and stopped sampling when 4096 cells have been open once.

B. Front-end Analog Circuit

The preprocessing of the PMT signals includes circuit-to-voltage converter, single-end to LVDS converter and offset adjusting. As is shown in Fig. 4, the charge signal from PMT is DC-blocked by a capacitor and converted to a voltage signal via a resister. The analog buffer consists of two separate high-speed amplifiers with high bandwidth. The first amplifier performs a voltage following circuit to achieve high input impedance. The second amplifier (THS4508) performs conversion from sing-ended to differential signalsand adds 6 dB gain. Two DC-blocking capacitors following the second amplifiers are used to deal with the common voltage to protect the input of DRS4. A DAC supplies individual DC offset for the differential input lines of DRS4 so that the input signals can accord with the linear range of DRS4.

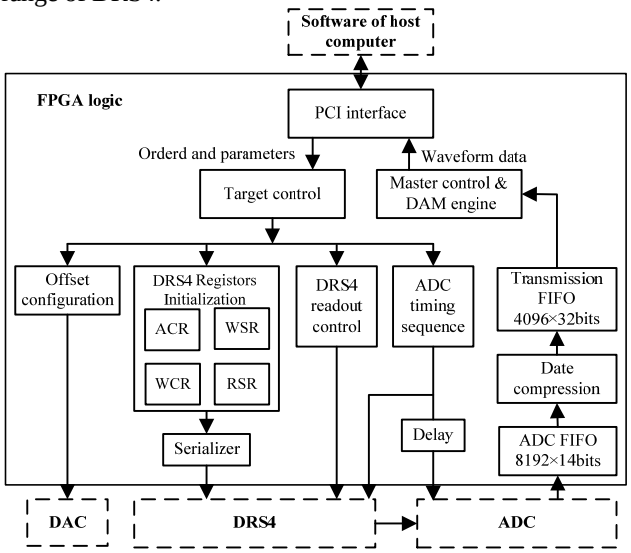

Figure 5. Logic of waveform digitization in FPGA.

C. FPGA Logic

The FPGA logic shown in Fig. 5 includes configuration, sampling and readout controller and data transmission. The configuration logic controls the DAC to generate offset voltages in order to adjust the DRS input and output offset and the sampling speed. Every second the offset voltages are calibrated depending on the temperature measured by the temperature sensor (MAX6662). After power-up, the configuration logic initializes the DRS4 registers which control the sampling mode (continuous cycling or single shot), channel switching and cascading. Then sampling and readout controller starts the DRS4 sampling at receiving external trigger and waits for the automatic ending of DRS4. The controller supplies the timing sequence of chosen readout mode (full read mode or region of interest read mode). The readout clock is 33 MHz generated by the PCI system clock and on-chip PLL of FPGA. For the best linearity, a strict phase difference between the waveform readout clock of DRS4 and the digitization clock of ADC is kept[7]. The digitized outputs of ADC are stored in a 14-bit

FIFO and then packed and compressed for delivery to PC. The data transmission is based on PCI interface in burst mode with a rate up to 20 Mbps. The software with a graphical user interface is developed based on Visual C++ and WINDRIVE which make the software design easier. The waveform will be fitted and calibrated. Then the integral area, TOF and fall time will be calculated.

III. CONCLUSION

The waveform digitizing module has been assembled and debugged with a signal generator. The debugging result shows it is able to acquire data of fast waveform. Now the module is waiting for in-beam nuclear experiments which are critical for testing the functional reliability. If the waveform digitizing module satisfies the experiment requirements, it will be copied to build a multichannel DAQ system. The system will used in the neutron detector to replace the old electronics composed of charge integrating circuits and TDCs.

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