Design of Handheld Test Equipment For High Performance Network over Coax

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***Abstract*—In this paper, we describe the design of handheld testers for HINOC (High Performance Network over Coax), which is a coaxial cable network access system self-developed by China. The HINOC handheld testers integrate the functions of modem and terminal. We mainly discuss two designs of HINOC handheld testers, namely single CPU architecture and dual CPU architecture, including hardware, software and the comparison between the two designs. The test results are shown at the end of the paper. Both designs of testers show good performance.**

Keywords-HINOC; broadband access; test equipment; design; embedded; architecture; handheld;

I. INTRODUCTION

HINOC (High Performance Network over Coax) system is a coaxial cable network access system self-developed by China, by using the external band resource of cable television to achieve the high performance of duplex information transmission.

Even HINOC is China's independent intellectual property rights of broadband access technology, there is no professional test equipment for it.

In the project construction of HINOC system, it needs some equipments to test the linking properties of HINOC network, including real-time network performance, system connection parameters, helping engineers solve the problems of network routing and system debugging. It is expected that in the next ten years, there will be massive application of HINOC systems, and large demand for test equipments. Based on this consideration, it is necessary to develop a commercial test equipment which is easy to take and operate, visual displaying and low cost. Therefore, we put forward the design scheme of HINOC handheld tester.

II. FUNCTION AND CHARACTERISTICS

The overall framework of HINOC system is shown in Fig.1. The two most important components of HINOC system are head device (HINOC Bridge, simplified as HB) and terminal device (HINOC Modem, simplified as HM). There are two major functions of HB: one is to connect the end of optical equipment through fiber, acting as the only transmission interface to optical device. The other is working as the central control unit of HINOC network to manage all of the HM devices within the network. The HB usually locates in the access point of residential areas, as a switch bridge between area network and core network. The HM usually locates in the user's house or building floor. One end of HM connects to HB through coaxial cable while the other end connects to TV, PC or other kinds of terminals.

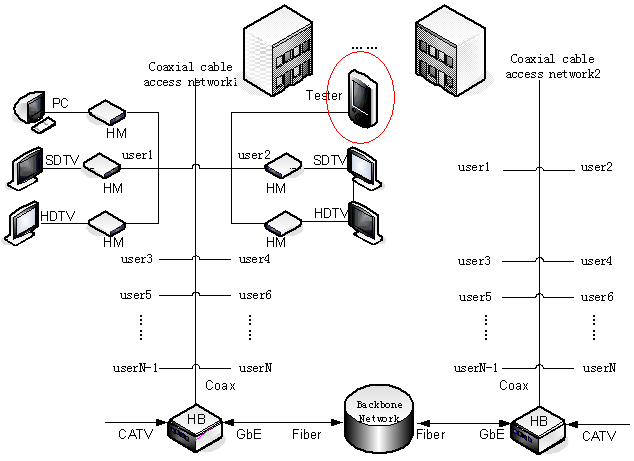

Figure 1. HINOC system schematic diagram

HINOC handheld test equipment provides visual testing method for engineers. It can acquire the physical layer, MAC layer and network layer data of HINOC communication system for checking the system fault. To simplify users' operation, necessary processing, analysis and display of the collected data are needed, which will be easier for users to set the functions of the equipment.

At the same time, the handheld tester integrates the characteristics of modem and terminal. It can be used as a HM modem in HINOC network and also supports terminal functions. It supports the intuitive interface of high resolution color touch screen. With USB host interface, it is to realize the test data storage. We mainly discuss two designs of HINOC handheld testers, namely single CPU architecture and dual CPU architecture.

III. HARDWARE ARCHITECTURE

A. Single CPU Hardware Architecture

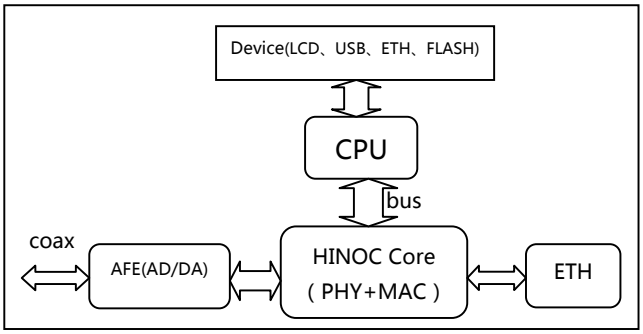

Figure 2. Single CPU hardware architecture diagram

The single CPU hardware architecture is shown in Fig. 2.In single CPU architecture, the modem function and terminal function of the tester are accomplished under the same CPU. The two main modules of the architecture are CPU core module and HINOC module.

1) CPU Core Module

The module core is XSCALE PXA270 processor, supporting Ethernet interface, serial ports LCD touch screen, and USB interface to realize terminal function. It connects with 32MB NOR FLASH and 32 MB SDRAM. The HINOC module and FPGA spectrum module are linked together with the CPU via data and address buses to realize its HINOC modem function.

2) HINOC Module

The input/output signal (in the same coaxial cable) of HINOC module is intermediate frequency signal. After AD/DA conversion by HINOC AFE circuit, it experiences data processing at the physical layer and MAC layer inside HINOC core chip. In the end, it realizes HINOC signal modulation and demodulation under the control of CPU PXA270.

B. Dual CPU Hardware Architecture

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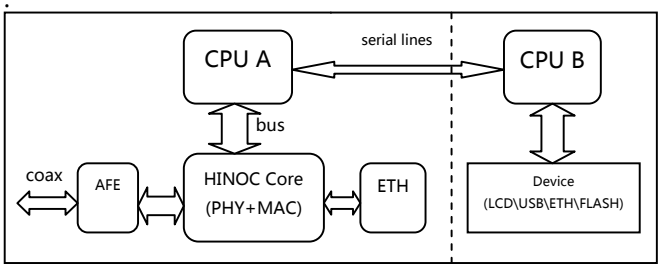


Figure 3. Dual CPU hardware architecture diagram

The dual CPU hardware architecture is shown in Fig. 3. The function of HINOC module is the same as single CPU architecture, which is to realize the physical layer and MAC layer processing. The CPU A connects to HINOC module through data and address buses, and then it realizes HINOC modem function. The CPU B is responsible for the realization of terminal function and controls of external devices such as LCD touch screen, Ethernet, USB and memory. The CPU B reads and writes HINOC parameters from CPU A via serial lines, and displays parameters on the touch screen in the forms of chart, curve or graph.

C. HINOC Modem Implementation

Whether it is single CPU architecture or dual CPU architecture, its HINOC modem function is realized through the interaction of HINOC module and CPU. When the HINOC intermediate frequency signal passes through AFE chip, the HIPHY module (which is the physical layer part of HINOC chip) will divide it into control signal and data signal. The control signal will be submitted to the CPU directly, but the data signal will continue to be packed or unpacked in the HIMAC module (which is the MAC layer part of HINOC chip) and then be submitted to the Ethernet interface. In the modem architecture, CPU is only responsible for the processing of control signal, the data flow doesn't pass through CPU. In this way, the burden of CPU is greatly reduced and data process speed and efficiency are greatly increased. The Fig. 4 below shows the HINOC modem architecture.

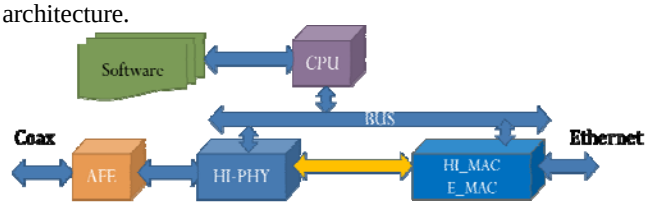


Figure 4. HINOC modem diagram

IV. SOFTWARE ARCHITECTURE

The software architectures of both single CPU and dual CPU handheld testers are divided into the kernel layer and the application layer. The realization of kernel layer is of the same mechanism.

A. Kernel Layer Structure

Considering the adaptability of different hardware platforms, the kernel layer is divided into the hardware access layer and the software platform during the realization process. Hardware access layer is mainly responsible for interaction with hardware platform and provides a common interface for software platform which is irrelevant to hardware. In this way, it separates the realization of software platform from specific hardware, enhancing the portability of the entire software platform. If the hardware platform is upgraded or changed, we only need to modify the hardware access layer codes and transplant the whole software platform. Therefore, the program codes of software platform can be well reused in other linux embedded systems which have similar functions with the handheld tester.

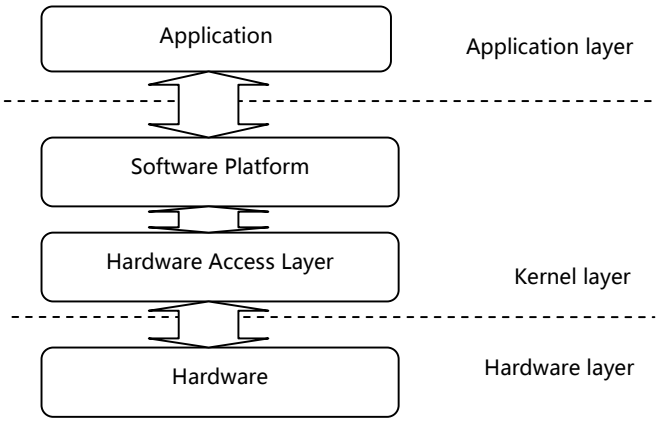


Figure 5. Kernel layer structure diagram

1) Hardware Access Layer

The hardware access layer is located in the kernel driver, and above the hardware layer. It provides an interface to access the hardware for the MAP control sub-layer, data convergence sub-layer and public department sub-layer upward. At the same time, it realizes the data transmission and control function by definition of standard interface to control hardware downward. The hardware access layer realizes specific operation according to specific hardware, but defines the same standard hardware operation interface such as interrupt, register read/write, memory operation for the sub-layer upward, so that the kernel driver is clear in structure and easy to transplant.

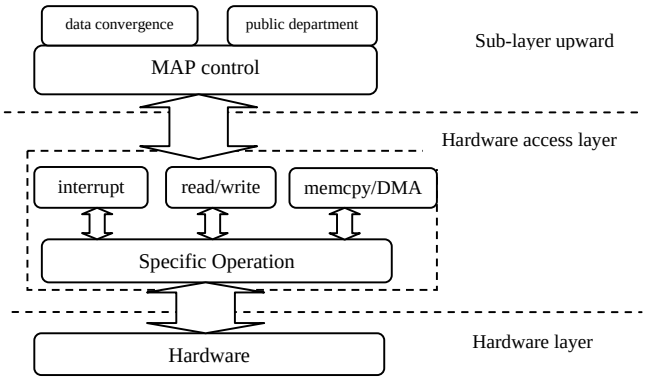


Figure 6. Hardware access layer structure diagram

2) Software Platform

The main part of the software platform is the HINOC network protocol stack. It will be added with some other device drivers such as FPGA read/write driver, touch screen driver and I2C driver according to specific demands. HINOC network protocol processing structure diagram is as follows:

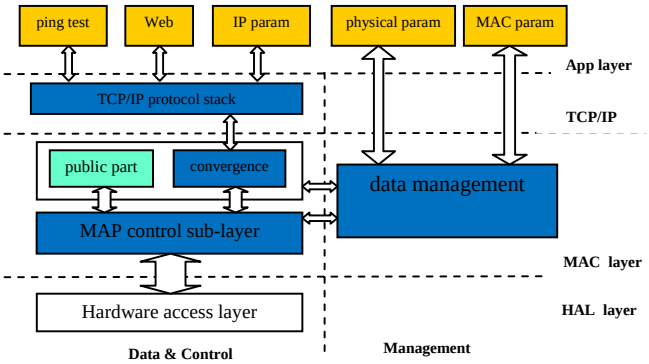


Figure 7. Software platform structure diagram

The software platform includes the MAC layer and the TCP/IP protocol stack. It gets data from the hardware access layer, then manages the data, provides parameters and network data for the application layer.

B. Application Layer Structure

The main application program is the Qt graphical interface displaying on the touch screen. An application layer interface is added between the Qt interface and the kernel, which is used for Qt program to call kernel functions. It also enhances the portability of Qt interface, which can be transplanted on different operation systems such as Linux2.4, Linux2.6, Linux3.0 easily. The Qt interfaces are the same in single CPU architecture and dual CPU architecture, but there is difference between the application layer interfaces.

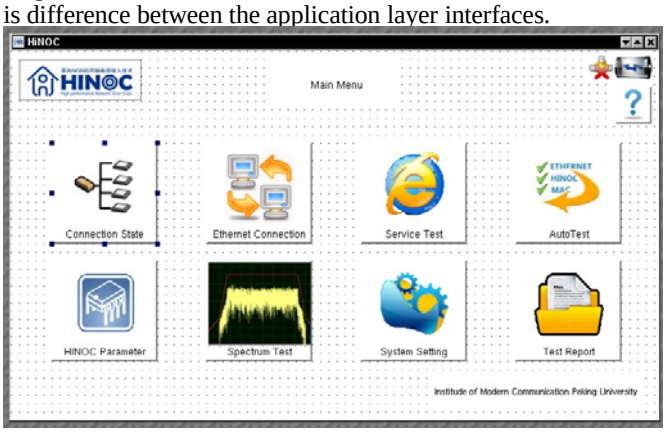


Figure 8. Main menu of Qt graphical interface

1) Application Layer Structure of Single CPU Arch

As it is shown in Fig. 9, the application layer interface of single CPU architecture gets IP layer data from the TCP/IP stack and gets physical or MAC parameters from the data management part of HINOC network driver.

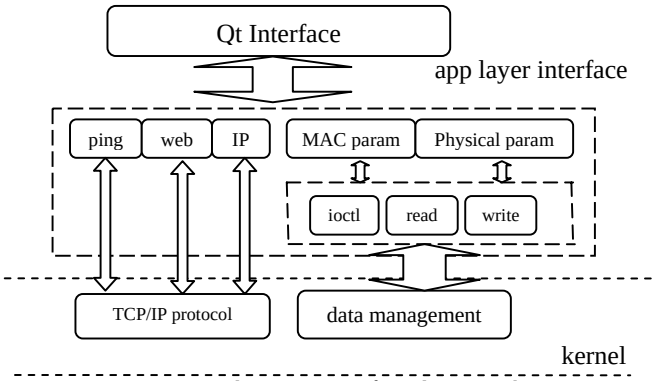
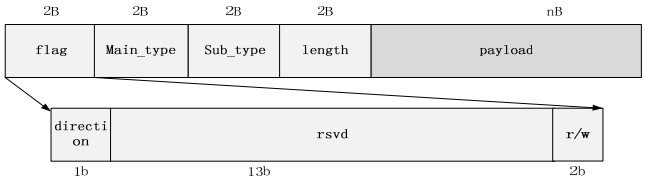


Figure 9. App layer structure of single CPU arch

When users open the Qt interface, the network driver device will be opened first. If the user clicks the physical menu, the application layer interface will call the ioctl function of kernel driver. The example is as the code below:

ioctl(fd,A270_SNMP,buffer);

One of the buffer frame structure of ioctl function is defined as follows:



We get corresponding function values through the buffer load domain by assigning type values to the buffer frame variables. By calling ioctl function, application layer interface provides Qt interface with physical and MAC parameters.

2) Application Layer Structure of Dual CPU Arch

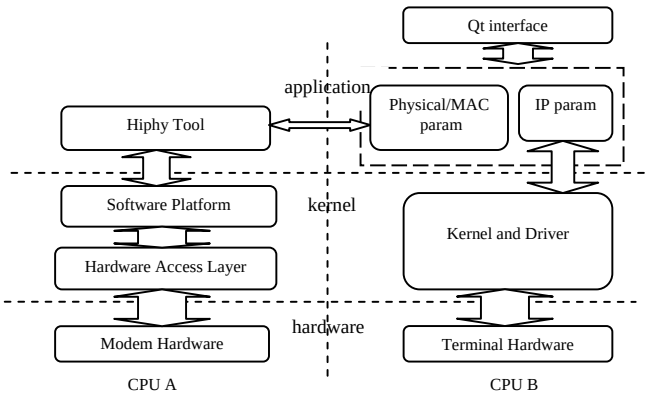


Figure 10. App layer structure of aual CPU arch

The application layer interface of dual CPU architecture accesses to HINOC network driver by the means of serial communication indirectly. In CPU A, there is a tool called Hiphy which can access to the HINOC kernel network driver directly. The Hiphy tool integrates with read/write, control and debug function about the HINOC network device. Therefore, in CPU B, application layer interface communicates with CPU A through the serial port and calls Hiphy tool functions to get physical and MAC layer parameters indirectly. It also gets IP parameters from the TCP/IP stack of CPU B's Linux kernel, and then submits all the parameters to Qt interface.

V. COMPARISON OF TWO ARCHITECTURES

The advantages and disadvantages of the two architectures are as follows.

In dual CPU architecture, CPU A is assigned with the HINOC modem function and CPU B the terminal function. Compared with single CPU architecture, each CPU in dual CPU architecture gets smaller task load and the response speed of overall system is faster, and the two CPUs can be well integrated for work. The terminal is mainly responsible for interacting with humans. Therefore, it should receive more attention for user experience and graphic design of display interface. It will highly require the whole hardware and software system to be upgraded for the terminal. For the dual CPU architecture, the HINOC modem and terminal are relatively independent, so it is easier to upgrade the terminal part of the whole system and keep in pace with the user demands. But for single CPU architecture, terminal upgrading will effect changes to the entire system. It will be much more complicated and cost more time and money than dual CPU architecture.

Although it is inconvenient to upgrade the single CPU architecture, the cost of the whole hardware system is lower because it integrates the modem and terminal functions in the same CPU. The choice of these two architectures depends on factors such as overall cost, necessity for upgrading and so on.

VI. RESULTS AND CONCLUSION

The hardware circuits of the two architectures are shown as below:

Figure 11. Single CPU circuit Dual CPU circuit

In the real test, hand-held tester (right machine box of the figure) and HB (left black box of the figure) are connected through coaxial cable. The test scene is as follows:

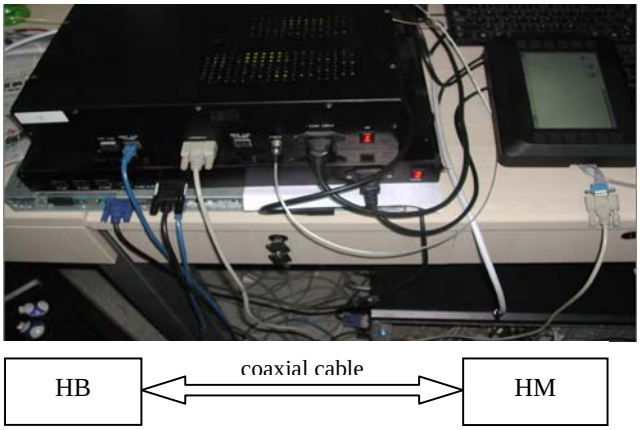


Figure 12. Test scene

The display interfaces of the two architectures are exactly the same, and some screenshots of test results are as follows:

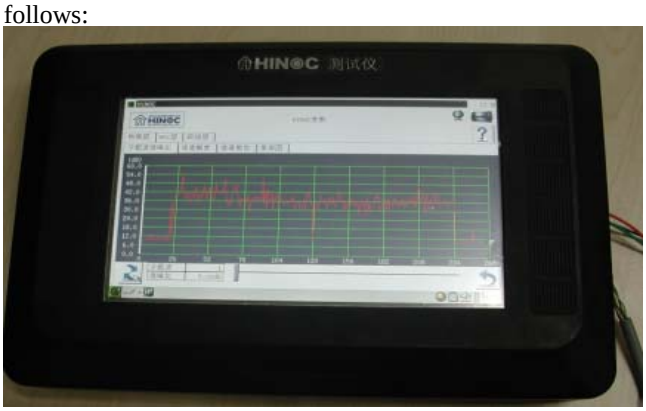


Figure 13. Physical SNR test screenshot

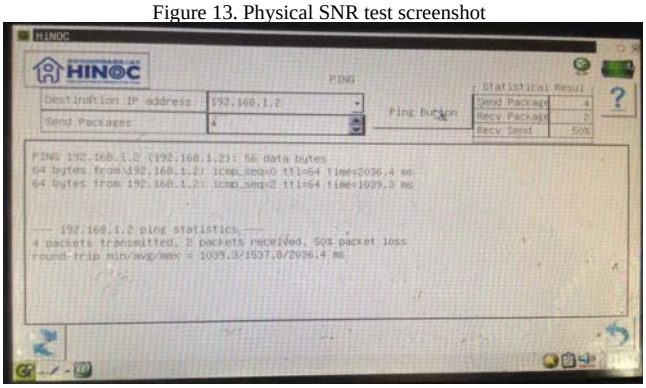


Figure 14. Ping test screenshot

From these test results we can see that both single CPU architecture and dual CPU architecture can display the Qt interface very well. Both kinds of the handheld testers are easy to operate , display visually and show good stablity. The physical layer, MAC layer and IP layer parameters are all displayed on the touch screen directly and vividly. And we can spot the problem with the HINOC network system easily with the help of a handheld tester.

The touch screen of current handheld tester is not sensitive enough, but it is enough for workplace usage. This problem will be well dealt with in the new version of handheld tester.

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