Research and Design of the DSRC device Measuring Instrument

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Abstract-**Along with an increasingly wide utilization in the fields of ETC application, it becomes more and more important to measuring quickly and accurately on the key equipment of ETC system, such as OBU and RSU . This article is based on the measuring requirement of ETC system and propose a new design proposal by selecting STR715FR0 chip base on the core of ARM7TDMI series and 5.8GHz radio frequency transceiver circuit, the actual operation and test results show that the DSRC device Measuring Instrument works with stability, reliability and low power consumption, which enables convenient and efficient measuring to ensure the reliability and consistency of the ETC key equipment.**

Keywords-ETC; DSRC;5.8GHz Transceiver; Measuring Instrument

I. I. INTRODUCTION

As the ownership of vehicles and flow has been increasing rapidly with economy's spring up in our country, the conflict comes out of the development in transportation infrastructure construction between the ownership of vehicles and flow. On account of the vehicle flow being beyond capacity of present transportation infrastructure construction, traffic jams come along and cause bad influence to economy .ETC(Electronic Toll Collection) show up as a effective settlement to above problem and widely spread over the world[1] [2] .It gives full play and improves the existing traffic resource utilization rate ,reduces the cost of transportation facilities .The ETC project has been developed by setting up ETC lane in many highway toll station during years since the 90s ,and the Wuhan city opened up the ETC project on urban area of road and bridge on July 1 this year .To ensure the Smooth implementation and guarantee the interconnection and interflow of ETC equipments produced by many factory under the national standard ,it requires a simple and portative detector to testing the ETC key equipment . This thesis discuss a DSRC device detector on testing RSU and OBU .The test can tell whether the equipment matches the national standard ,the road charges management department and consumers' demand .

II. II. THE FEATURE AND SYSTEM ARCHITECTURE DESIGN

2.1 The feature of DSRC device Measuring Instrument
1)Monitor: It can receive and demodulate the signal from RSU and OBU, Monitoring the   communication process of RSU with OBU, observed in the format and quality of the communication data, verify the data link layer of the time window parameter;

2)Protocol test: FM0 decoding and HDLC decoding communication data, to analyze baseband data, confirm the format and content of the data to meet the protocol requirements

3)Wake-up sensitivity measurements:The instrument can transmit a 5.8 GHz RF signal, simulate the OBU required "14K+BST" wake-up signal, used to wake OBU.And the wake-up signal transmitted power is adjustable, in order to test the OBU wake sensitivity

4)The developed instrument has miniaturized design, portable operation.

2.2 The system architecture of DSRC device Measuring Instrument

The major system architecture of DSRC device measuring Instrument consists of hardware and software components.

The figure 1 shows the hardware system structure. The hardware mainly have two parts: a RF circuit and a control circuit.The RF circuit   comprises a radio frequency transmitter circuit, a radio frequency receiver circuit, a transceiver antenna and a T/R switch. The control circuit includes a lower machine and a host computer. Lower machine use MCU to complete the RF circuit control, generate the transmitting baseband data, receive demodulated data and decode, responsible for communication with the host computer. The host machine selects a portable Tablet PC,to complete human-computer interaction and interface display and lower machine communication.

The signal from antenna filter out-of-band interference signal through radio frequency band-pass filter, and then amplified by Ultra-wideband Low Noise Amplifier. The amplified signal mix with hopping local oscillator signal generated by VCO to convert signal to fixed mid-frequency after through filter .Then convert signal to digital signals through mid- amplifier and detection of IF filter. Finally upper computer display the signal transmitted from serial port after through low- amplifier and data parse of filter.
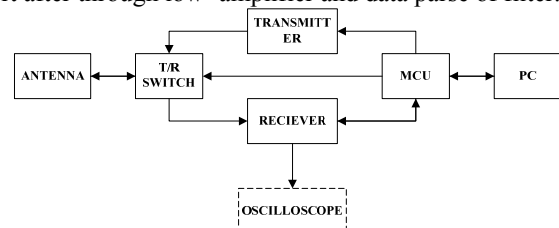

Figure 1: The hardware system structure

The hardware part consists of radiating circuit, receiving circuit, A/D conversion circuit. The radiating circuit mainly works for BST modulation to making it awake OBU in case of testing OBU with RSU's absence. The receiving circuit receive signals from OBU and RSU, detect baseband signal through mixing. The A/D conversion circuit parse baseband signal to get digital signal.

The software part consists of four parts. The first part is used to generate BST signal by single-chip system to awaken OBU. The second part parse baseband signal in A/D conversion circuit after detection. The third part program MCU to different local frequency output by controlling the input voltage of voltage-controlled oscillator. The forth part program software to display the parsed data on the computer.

This text would not involve specific software programming.

III. THE DESIGN OF HARDWARE

The hardware part consists of antenna, power-module, launch/receive circuit, A/D conversion circuit, local frequency circuit.

3.1 Antenna module

Some antenna can be used as duplexer in this frequency such as paraboloid antenna, spiral antenna, ring antenna, dipole antenna, aperture antenna and microstrip antenna. Paraboloid antenna and spiral antenna are too thick to fit miniaturization, and ring antenna and dipole antenna has disadvantage on directionality, so we choose aperture antenna and microstrip antenna as duplexer.

3.2 Transmitter module

The RF chip of DSRC device detector is selected under consideration of the national standard, frequency point, modulation demodulation system, transmission rate and gain and other technical standard. After analysis, this design turn out to be consist of 5.8GHz oscillator, ASK signal modulation circuit, band-pass filter, RF power amplifier and transmitting antenna.
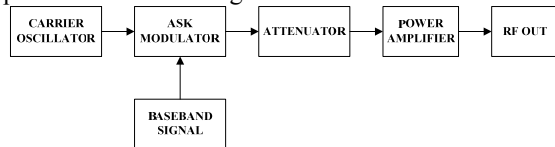
Figure 2: The block diagram of transmitter circuit

The FM0 encoded base-band signal and 5.8GHz oscillator generated by MCU process ASK modulation and then use band-pass filter getting rid of LF noise and high order harmonic noise to get better SNR. Then system transmits signals via antenna after amplifying the modulating signal.

3.3 Receiver module

The receive module of DSRC device detector is composed of high power amplifier, filter, mix-frequency, local oscillator, middle power amplifier, detection and low power amplifier. According to the standard and demand, we select HMC476G 、 5800filter 、 HMC218 mixer 、 UPC1688G and UPC2710T making up middle power amplifier, detection and low power amplifier chips

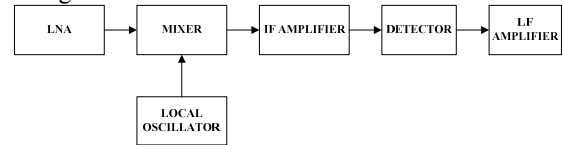MAX4212 together with peripheral circuit to form the receiving circuit.

Figure 3: The block diagram of receiver circuit
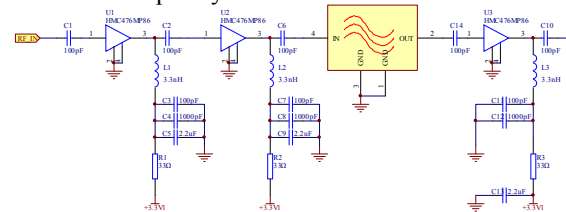
3.3.1 Radio frequency LNA circuit

Figure 4 Radio frequency LNA circuit

The Radio frequency LNA circuit consists of three HMC476 and 5800 filter. It can amplify signals from antenna by Level 3 high power low noise amplifier and output to mixer after band-pass filtering.
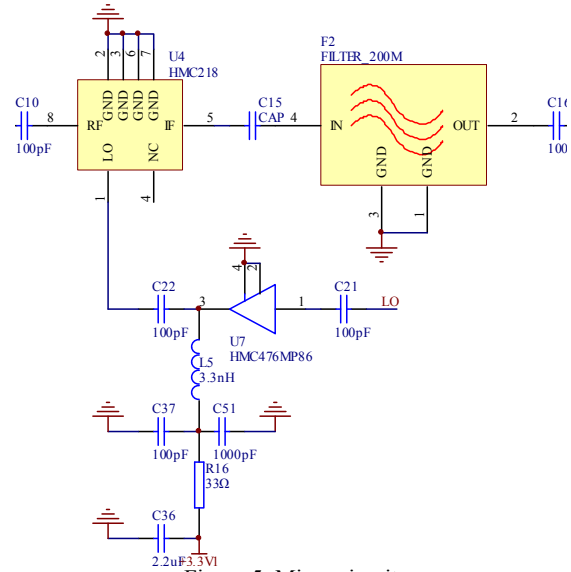
3.3.2 Mixer circuit

Figure 5: Mixer circuit

Mixer circuit composes of HMC218 chips. It convert received signal to base-band signal by mixing signal amplified via low noise amplifier with local oscillator. HMC218 has some characters, such as better performance as mixer.
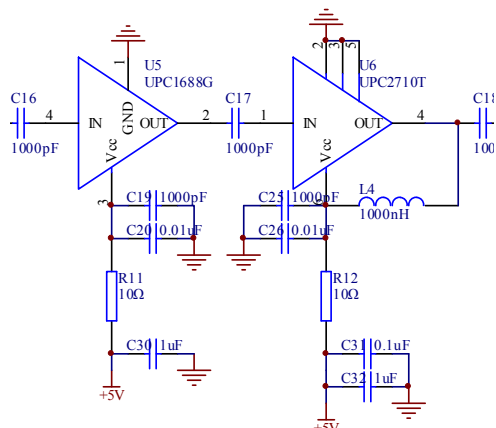
3.3.3 Middle frequency amplifier Circuit

Figure 6: Middle frequency amplifier Circuit

Circuit of middle frequency amplifier is made up of two amplifier chips UPC1688G and UPC2710T together with the required peripheral circuit which can generate maximum 54 db gain on the IF signal from mixer.
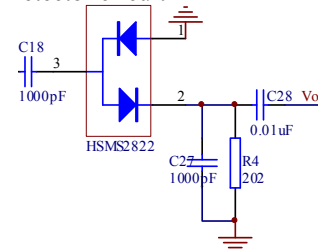
3.3.4　Detector circuit

Figure 7: Detector circuit

The HSMS2822 chip forms the mainly function of the detector circuit.
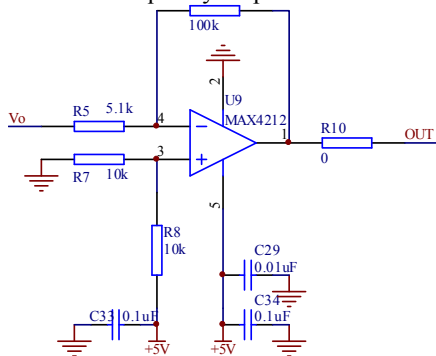
3.3.5　Low frequency amplifier circuit

Figure 8: low frequency amplifier Circuit

The MAX4212 chip and its peripheral circuit constitute the mainly function of the low power amplifier circuit. It amplifies the signal from detector and exports it to the A/D conversion circuit.
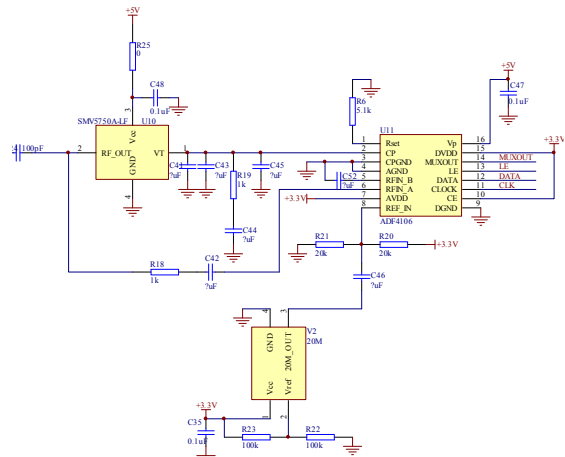
3.3.6　Local oscillator Circuit

Figure 9: Local oscillator circuit

Circuit of local oscillator consists of 20M crystal oscillator, ADF4106, SMV5750A.

ADF4106 is an integrated digital phase-locked frequency synthesis chip produced by ADI firm of America gathering low noise digital phase discriminator, programmable divider and precision charge pump. This chip advantages on the super high upper working frequency limit which can reach 6 GHz [7].

The export of SMV5750A can be controlled by MCU. The fine adjustment on oscillator according to practical demand becomes accessible due to the voltage controlled oscillator output frequency controlled by the VCO's voltage. This process optimizes system performance and reduces the cost.

3.4 Data decoding module

The data decoding module parses the digital signal from detector and sends it to upper computer to accomplish the display and process of upper computer software. As the key part of DSRC device detector, rapid processing capacity, low power, bigger memory capacity and higher reliability are required. In order to meet these requires, we choose the STR715FR0 based on the core of ARM7TDMI series produced by ST Microelectronics for its several characteristics showed as follow [5]

(1) STR715FR0 is a MCU for beginner, low cost and simplified internal resources

(2) It has16KB to 64KB FLASH and 16KB SRAM storage, but no CAN and USB modules.

(3) It has 32 I/O ports and 10 communication ports including 2 I2C (one multiplex with SPI), 4 UART asynchronous serial ports, smart card ISO-7816-3 port (multiplexing with UART1), 2 BSPI ports, HDLC synchronous communication port.

(4) The maximum system running speed can reach 50MHz clock frequency.

(5) A/D converter can achieve single channel or four channels' switch under single or continuous conversion mode.

IV.　CONCLUSIONS

As the ETC application has been more and more widely used, stable and reliable performance of OBU and RSU

becomes important guaranty for ETC system. According to the ETC test requirements, this text proposes a new design proposal and detailed hardware circuit diagram by selecting the STR715FR0 based on the core of ARM7TDMI series and its correlated HF transmit-receive circuit. As presented by test result and practical function, this designed DSRC device detector works stable and reliable, uses low power, realizes effective supply of convenient and efficient detection on ETC key equipment, and ensure the reliability and consistency of devices at factory or in use. Not only protecting the profit of road toll administration from wastage, it also makes device detecting time short and reduces some unnecessary trouble. As DSRC technology has been applied in more fields and detection for those devices is unavoidable, DSRC device detector is bound to bring huge convenience to intelligent transportation system.

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