Design of a dual-core Holter Systerm Based on STM32 and FPGA

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***Abstract*—ECG (electrocardiogram) currently is the most effective way to detect the heart condition. Previously people have to do the ECG recording in hospital. But the ECG abnormal situation is unsustainable, because the symptoms usually disappear when the patient is sent to the hospital. This may lead to losing the early treatment opportunity. In this paper, a Holter system is designed based on STM32 and FPGA dual-core. ECG data acquisition, LCD display, and data storage in SD card are accomplished. In addition, an ECG de-noised method which combines Stationary Wavelet Transform with Wavelet Transform Scale factor Estimate is accomplished on FPGA to eliminate the noise of ECG. The system can be used anywhere at any time, so it's an ideal device for remote health care.**

Keywords-ECG; FPGA; STM32; SWT; WTSE; de-noise

I. INTRODUCTION

Along with the rapid economic development as well as changes in lifestyle, cardiovascular disease has become one of the most important reasons that cause death recently. People may lose lives even when the heart doesn't work only for a second. ECG signal objectively expresses the heart activity and is a typical biological electric signal. The correct diagnosis of cardiovascular disease depends on the accuracy of ECG acquisition. ECG recorders are often called Holter recorders, named after the first ECG recorder developed by N. J. Holter in 1961[1].

ECG signal is a kind of very weak electrical signal whose amplitude is only 0.05mV-5mV, and the spectrum scope mainly focus on 0.05 ~ 100Hz[2], so it's often drowned in Strong Noise Jamming. Therefore ECG signal has a disadvantage of low signal-to-noise ratio (SNR). However we can't extract useful ECG characteristics from the distortion waveform, so restraining and removing the noise from ECG effectively is very important in ECG single processing.

The Holter recorder described in this paper is based on STM32 and FPGA dual-core. Taking as main processor, STM32 is used to manage the whole system, such as input scan, wave display, data storage in SD card, and operate the FPGA. Taking as co-processor, FPGA consists a large number of programmable logic blocks, which can each implement an amount of digital logic, and have a high execution speed, so FPGA is used to run the filtering algorithm to meet the requirements of real-time processing, the Analog-to-digital converter module is also operated by FPGA. Two cores are connected by Parallel bus.

II. HARDWARE DESIGN

In the acquisition system, the hardware consists of electrodes, amplifier circuit, Analog-to-digital converter module, FPGA, STM32, SD Card and LCD module. The system-level description is shown in Figure1.

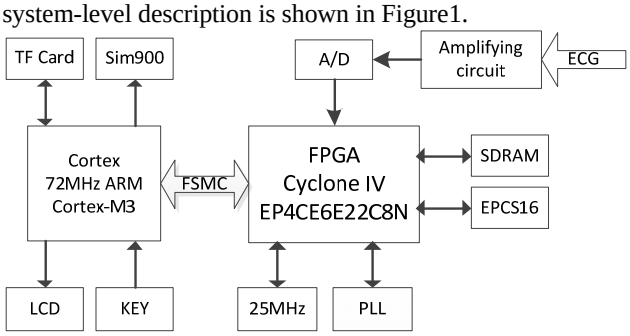


Figure1. The system-level description

A. Amplifier and Analog-to-digital converter module

In the amplifier and analog-to-digital conversion circuit, the ECG signals are collected by electrodes attached to human body. The system adopts 1-lead system. In the acquisition of ECG, the right leg electrode (RL) is generally as reference electrode, right arm electrode (RA) and left arm electrode (LA) output ECG. The amplitude of ECG is only 0.05mV-5mV, so higher requirements are needed for pre-amplifier.

The amplifier circuit designed in this paper covers voltage follower, amplifier circuit, right leg drive circuit and shield drive circuit in order to suppress noise interference and increase signal to noise ratio (SNR). The circuit uses low-cost and high-precise instrumentation amplifier AD620[3] and low-power quadruple operational amplifiers TLV2254[4] as core devices. Stronger ECG can be obtained with the help of voltage follower and the issue of common

mode interference and the ECG device's electrical safety is solved by right leg drive circuit and shield drive circuit.TLC1549[5] are 10-bit, switched-capacitor, successive-approximation analog-to-digital converters, which could effectively save the port of controller because the data is transmitted serially and this chip has characteristics of CMOS process, conversion of high precision and strong anti-jamming capability. The amplifier circuit design is shown in Figure2.

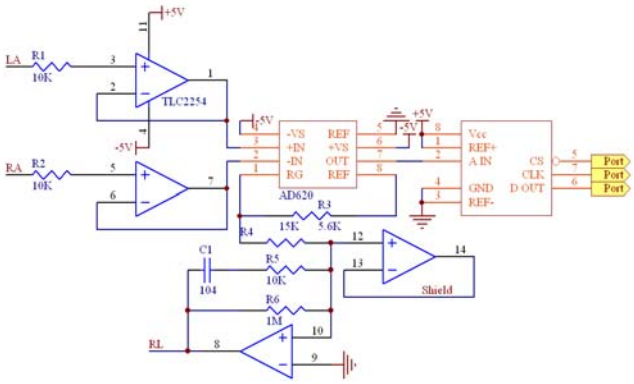


Figure2. The amplifier circuit schematics

B. STM32

The STM32F103VC [6] is based on ARM Cortex™-M3 which is a High-density performance line ARM-based 32-bit MCU with 256KB flash and 64KB SRAM. The STM32F103VC covers all common peripherals, including serial, I^2C, SPI, CAN, Ethernet, and most of them are connected to the DMA controller. Flexible Static Memory Controller (FSMC) as a new feature is contained. In this paper, STM32 takes as main processor, and is used to manage the whole system.

C. FPGA

Altera's new Cyclone™ IV FPGA device family extends the Cyclone FPGA series leadership in providing the market with lowest-cost, lowest-power FPGAs. The EP4CE6E144P2 is part of the family, with 15 multipliers, 2 PLLs [7]. 8M SDRAM and 2M flash are added as external memory. FPGA contains a large number of programmable logic blocks, which can each implement an amount of digital logic, and have a high execution speed, so in this paper FPGA is used to run the filtering algorithm to meet the requirements of real-time processing, the Analog-to-digital converter module is also operated by FPGA.

D. Flexible Static Memory Controller

The FSMC is embedded in the STM32F103VC, which has four chip select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND. It can send the corresponding types of data or control signals depending on the type of external memory by register setting. The FSMC can be configured in the form of seamless interface with most graphic LCD controllers. It supports the Intel 8080 and 6800 modes. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration. The Holter recorder described in this paper uses FSMC to control the LCD and FPGA, and the mapping address start from 0x6080 0000 and 0x6000 0000.

III. SOFTWARE DESIGN

The software design of the system contains two parts which act on STM32 and FPGA. The FPGA is programmed with Verilog. Firstly TLC1549 is operated by FPGA to get Digitized ECG date; then data is sent to filter, and FPGA sends de-noising signal to STM32.The code of the STM32 is programmed with C. The first work the STM32 should do is init the system; an enable signal is send to FPGA, LCD and SD Card. Then STM32 read data from FSMC; the new data is saved to SD Card, and the last 200 data are drawn on the LCD.GUI is used to facilitate interface in the design. The flowchart of system software is shown in Figure3.

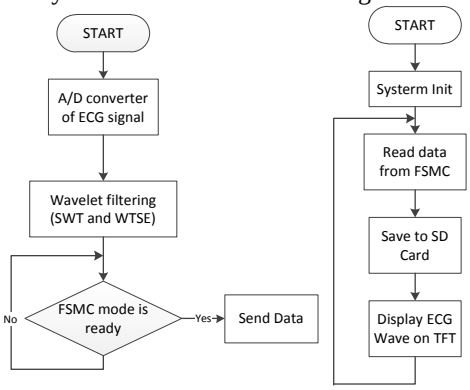


Figure3. Block diagram of the system software

A. SWT and WTSE

There are many methods in de-noising of ECG but have different effects in filtering result, complexity and speed. Low pass filter[8] is effectively in restraining high frequency noise with simple filter structure, but its greatest shortcoming is also can restrain the other useful ECG signal. Mallat [9] is also called the pyramid algorithm based on multi-resolution analysis, is the fast algorithm of wavelet transform, which can restrain the high and low frequency interference effectively, but obvious Gibbs phenomenon will appear in signal reconstruction. Median filtering[10] is good at restraining baseline drift inhibition of ECG, but should adopt large filtering window in removing low frequency noise, which leads to occupy too much comparator resources and having difficulty in realization.

Stationary wavelet transform (SWT)[11] not only can retain advantages of multi-resolution analysis but also can suppress the Gibbs phenomenon effectively, but will occupy more storage. Stationary wavelet transforms insert zeroes between filter coefficient rather than doing down sampling on subbands at each level. The calculation process of coefficient is shown inFigure4.

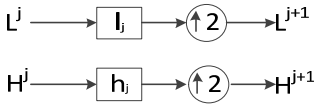


Figure4. The calculation process of coefficient

If $f_{(t)}$ express the original signal sequence, $A_D = f_{(t)}$, $L^D = L$, $H^D = H$, stationary wavelet transform is shown as below:

$$A_{j+1} = L^j A_j \quad (1)$$

$$D_{j+1} = H^j A_j \quad (2)$$

Wavelet Transform Scale factor Estimate (WTSE)[12] is a way that makes one of the subbands at high level as an approximation of low noise in ECG, so it's good at restraining baseline drift and the complexity of hardware is lower. In this paper a filter is designed in the way that combines SWT with WTSE.

B. Implementation on FPGA

In this design, Harr wavelet is selected, because the num of filter coefficient is 2,even though the number of each layer filter coefficient is twice as the upper layer, but the multiply-add operation is effective with only two non-zero coefficient participation, so the complexity of hardware realization is low. In order to meet the requirements of real-time processing two RAM buffer are added to the design. Figure5 shows the flow chart of algorithm implemented.

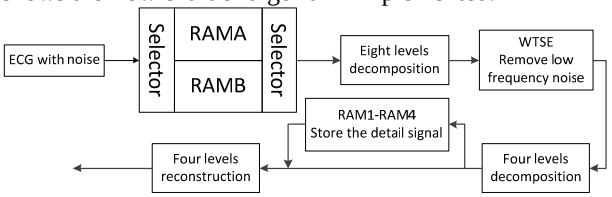
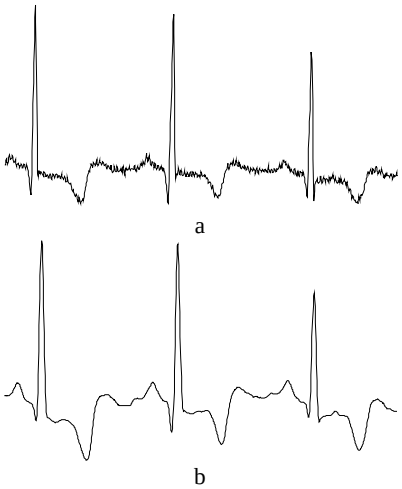


Figure5. The flow chart of algorithm implemented

IV. RESULTS

In order to test the effect of signal processing in this design, four sets of data in MIT-BIH ECG database, 100.dat, 103.dat, 112.dat 114.dat are selected to test. Figure6-Figure9 show the experimental result, a represent the original signal, b represent the output of the system. Figure10 shows the design display interface, and ECG collected from the body is displayed.

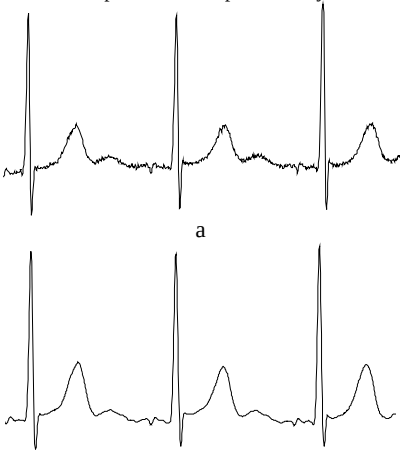


a

b

Figure6. 100.dat filtering effect comparison

a represent the original signal
b represent the output of the system

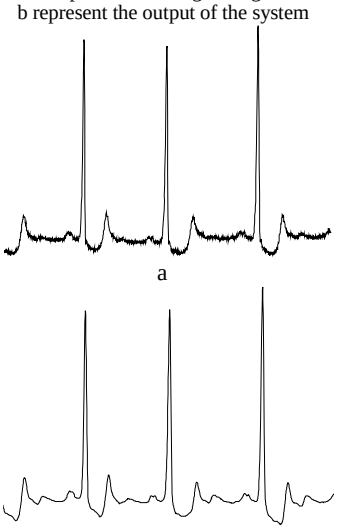


a

b

Figure7. 103.dat filtering effect comparison

a represent the original signal
b represent the output of the system

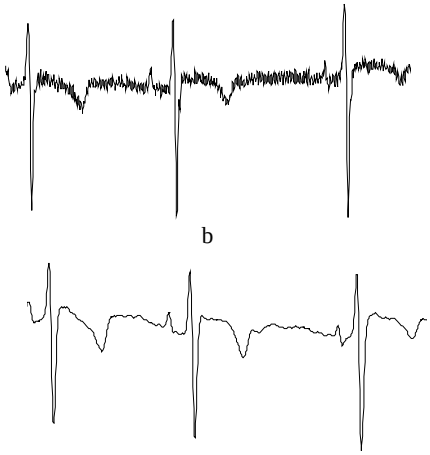


a

b

Figure8. 112.dat filtering effect comparison

a represent the original signal
b represent the output of the system



b

b

Figure9. 114.dat filtering effect comparison
a represent the original signal
b represent the output of the system

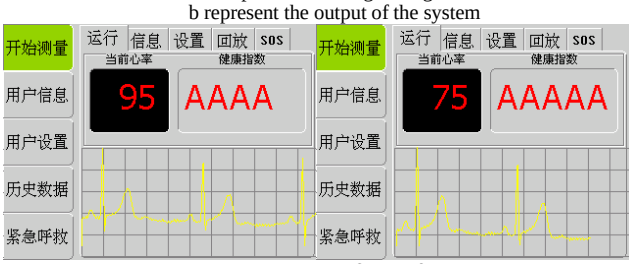


Figure10. Display interface of the design

V. CONCLUSION

A new Holter system is designed based on STM32 and FPGA, including ECG acquisition, signal de-noising, LCD display, and data storage in SD card. The filter design method combining SWT and WTSE is a new method, the de-noising effect and the speed could meet the requirements of Holter. A friendly interface is developed and the system operates simply, so it would be ideal ECG monitoring equipment.

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