A Threshold Voltage Model for the IMOS Device Using Hetero Structure

Heming Yao[a]
a Beihang Sino-French Engineer School，
Beihang University,
Beijing, China
yaoheming2010@yahoo.cn

***Abstract*—IMOS allows very sharp subthreshold slopes, even down to a few mV/dec at room temperature. However, the device has serious reliability problems, such as large threshold voltage shifts, caused by hot carrier induced damage and the large supply voltage. Hetero IMOS, using the small bandgap material as the channel material, improves device reliability and decreases power consumption by reducing off-state currents and features a lower breakdown voltage compared to conventional IMOS. In this paper, a threshold voltage model is proposed in different distribution of surface electric field and in the condition of avalanche breakdown. The result is analyzed with the simulation data. It promotes the application of IMOS to VLSI design.**

Keywords-avalanche breakdown; Hetero IMOS; threshold voltage

I. INTRODUCTION

While the feature size of MOSFET devices is reaching its physical limits due to several phenomena, such as the high subthreshold swing [1], the thermal diffusion of carriers at low gate voltages and the short channel effect [2], IMOS is receiving an increasing amount of attention. IMOS, proposeded for the first by Gopalakrishnan et al. [3] in 2002, is able to reach subthreshold slopes as small as 5mV/dec at room temperature [4]. However, some problems of IMOS, such as the relatively high operating voltage and power consumption, are never ignored due to their negative influence on its reliability. A germanium based device was analyzed by Gopalakrishnan et al. to improve the performance of IMOS [5]. However, there are still many technological barriers to fabricate practical germanium devices [6]. Although a single gate IMOS structure [7], using SiGe-On-Insulator technology (SG-SGOI IMOS) and employing $Si_{1-x}Ge_x$ as a channel material, leads to significant reduction in supply voltages. However, this technique results into an increase in on-state current. Hetero IMOS [7], equipped with with Si/Si-Ge channel, has a lower breakdown voltage, and reduces the operating voltage and power consumption of devices.

In this paper, a model for threshold voltage of Hetero P-IMOS is developed by resolving the 2D Poisson equation and in the condition of avalanche breakdown. By analyzing the model, the reliance of threshold voltage on the drain-source voltage, on the silicon-cap layer thicknesses and on the gate length is studied, respectively. The results of the models are in good agreement with that of simulation.

II. HETERO IMOS STRUCTURE

The basic device structure of the Hetero IMOS is a gated p-i-n diode Fig. 1, as that in the IMOS, except that the channel region employs the Si/Si-Ge channel. In this structure, on top of the $Si_{1-x}Ge_x$ layer is placed a silicon-cap layer. The overall thickness of this layer and the $Si_{1-x}Ge_x$ layer is equal to the thin-film thickness of the device.

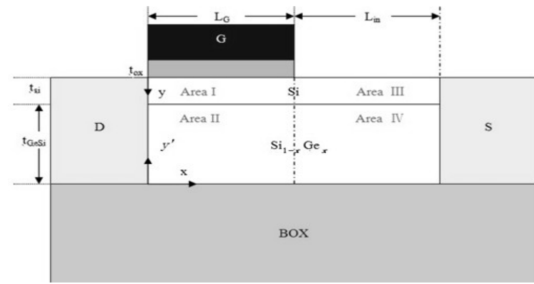

Figure1. Cross section of the Hetero P-IMOS

III. THRESHOLD VOLTAGE MODEL

The input parameters used for the Hetero P-IMOS are indicated in the Fig. 1. The gate voltage, which leads to the avalanche breakdown, is called the threshold voltage [8]. The distribution of the electric field is firstly analyzed to derive the threshold voltage model. The device is divided into four different parts Area I, Area II, Area Ⅲ and Area Ⅳ. The threshold voltage of the IMOS is controlled by gate voltage and source-drain voltage, so the 2D Poisson should be used to describe the characteristics of Area I and Area II, before the strong inversion appears. The equations in the Area I and Area II can be written as:

$$\frac{\partial^2\phi_1(x,y)}{\partial x^2}+\frac{\partial^2\phi_1(x,y)}{\partial y^2}=-\frac{qN_A}{\varepsilon_{Si}},\quad (0\leq x\leq L_G,\ 0\leq y\leq t_{si}) \tag{1}$$

$$\frac{\partial^2\phi_2(x,y')}{\partial x^2}+\frac{\partial^2\phi_2(x,y')}{\partial y'^2}=-\frac{qN_A}{\varepsilon_{GeSi}},\quad (0\leq x\leq L_G,\ 0\leq y'\leq t_{GeSi}) \tag{2}$$

The potential in the vertical direction in the channel region can be approximated by a parabolic function, the equations are as follows:

$$\phi_1(x,y)=\phi_{s1}(x)+c_{11}(x)y+c_{12}(x)y^2,$$

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$(0 \leqslant x \leqslant L_G,\ 0 \leqslant y \leqslant t_{si})$ (3)

$$\phi_2(x, y') = \phi_{s2}(x) + c_{21}(x)y' + c_{22}(x)y'^2,$$

$(0 \leqslant x \leqslant L_G,\ 0 \leqslant y' \leqslant t_{GeSi})$ (4)

We hypothesize that 1) $t_{BOX} >> t_{si}$ and $t_{BOX} >> t_{GeSi}$; 2)the Substrate electrode links to the ground; 3) The oxide layers contain no impurity charge. The equations (1, 2) can be solved, by using the following boundary conditions:

$$[\frac{d\phi_1(x, y)}{dy}]_{y=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}(\frac{V'_G - \phi_{s1}(x)}{t_{ox}}) \quad (5)$$

$$[\frac{d\phi_2(x, y')}{dy'}]_{y'=0} = 0 \quad (6)$$

$$[\frac{d\phi_1(x, y)}{dy}]_{y=t_{Si}} = [-\frac{\varepsilon_{GeSi}}{\varepsilon_{Si}}\frac{d\phi_2(x, y')}{dy'}]_{y'=t_{GeSi}} \quad (7)$$

$$[\phi_1(x, y)]_{y=t_{Si}} = [\frac{\varepsilon_{GeSi}}{\varepsilon_{Si}}\phi_2(x, y')]_{y'=t_{GeSi}} \quad (8)$$

Substituting ϕ_1, ϕ_2 and substituting y = 0, we obtain the equations:

$$\frac{\partial^2\phi_{s1}(x)}{\partial x^2} - a_1\phi_{s1}(x) + a_2\phi_{s2}(x) = b_1 \quad (9)$$

$$\frac{\partial^2\phi_{s2}(x)}{\partial x^2} - a_3\phi_{s1}(x) + a_4\phi_{s2}(x) = b_2 \quad (10)$$

We substitute ϕ_{s2} with ϕ_{s1} in the equation (9), the result is as follows:

$$\frac{\partial^4\phi_{s1}(x)}{\partial x^4} - (a_4 - a_1)\frac{\partial^2\phi_{s1}(x)}{\partial x^2} - (a_1a_4 + a_2a_3)\phi_{s1}(x) = (a_2b_2 - a_4b_1) \quad (11)$$

In fact, the variation of $\phi_{s1}(x)$ is enough so smooth that the equation (11) could be simplify as the equation (12):

$$\frac{\partial^2\phi_{s1}(x)}{\partial x^2} - \alpha\phi_{s1}(x) = \beta \quad (12)$$

We can acquire the solutions:

$$\phi_{s1}(x) = A\exp(\sqrt{\alpha}x) + B\exp(-\sqrt{\alpha}x) - \frac{\beta}{\alpha} \quad (13)$$

The electric field distribution can be written as follows:

$$E_1(x) = -A\sqrt{\alpha}\exp(\sqrt{\alpha}x) + B\sqrt{\alpha}\exp(-\sqrt{\alpha}x) \quad (14)$$

As for Area Ⅲ and Area Ⅳ, 1D Poisson equation will be now applied to determine ϕ_{s3}, ϕ_{s4}, we obtain the equations:

$$\phi_{s3}(x) = -\frac{qN_A}{2\varepsilon_{Si}}x^2 + C_3x + D_3 \quad (15)$$

$$\phi_{s4}(x) = -\frac{qN_A}{2\varepsilon_{GeSi}}x^2 + C_4x + D_4 \quad (16)$$

The corresponding electric field distribution of the Area Ⅲ can be written as follows:

$$E_3(x) = \frac{qN_A}{\varepsilon_{Si}}x - C_3 \quad (17)$$

In order to determine the unknown element A, B, C and D, the following boundary conditions are used:

$$\begin{cases} \phi_{s1}(0) = V_D \\ \phi_{s3}(L_G + L_{in}) = V_S + V_{bi} \\ \phi_{s1}(L_G) = \phi_{s3}(L_G) \\ [\frac{d\phi_{s1}(x)}{dx}]_{x=L_G} = [\frac{d\phi_{s3}(x)}{dx}]_{x=L_G} \end{cases} \quad (18)$$

It has been proved that the avalanche breakdown happens firstly in the silicon-cap layer[3]. Therefore, to obtain a model for threshold voltage, we have to find the precise location of the maximum electric field from equations (14) and (17) by substituting the condition dE/dx = 0. The maximum electric field location will be obtained as $x_{max}=L_G$. When the electric filed in $x_{max}=L_G$, reaches critical electric field, the avalanche breakdown is triggered, the device is open. By substituting $x_{max}=L_G$ into (17), and use $E_3=E_{cri}$, the threshold model is written as:

$$V_{th} = \frac{(a_1 - a_4)\frac{\chi_1}{\chi_2} + \frac{a_4qN_A}{\varepsilon_{Si}} - \frac{a_2qN_A}{\varepsilon_{GeSi}}}{a_4\xi_2 - a_2\xi_1} - \Delta\varphi_{MI} \quad (19)$$

$$E_{cri} = \frac{qN_AL_G}{\varepsilon_{Si}} - C_3 \quad (20)$$

When we have:

$$\chi_1 = (r_2 - r_1)V_D\exp(\sqrt{\alpha}L_G) + \frac{r_2qN_A}{\varepsilon_{Si}}(L_{in}^2 + 2L_GL_{in}) - \frac{r_1qN_AL_G}{\sqrt{\alpha}\varepsilon_{Si}} + \frac{C_3r_1}{\sqrt{\alpha}} - r_2C_3L_{in} + r_2(V_S + V_{bi})$$

$$\chi_2 = \frac{r_1\exp(\sqrt{\alpha}L_G)}{\alpha} - \frac{r_2}{\alpha} - \frac{r_2\exp(\sqrt{\alpha}L_G)}{\alpha}$$

$$\xi_1 = \frac{2\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}} + \frac{\varepsilon_{ox}t_{GeSi}}{\varepsilon_{GeSi}t_{ox}}}{t_{Si}^2(1 + \frac{\varepsilon_{Si}t_{GeSi}}{\varepsilon_{GeSi}t_{Si}})}, \xi_2 = \frac{\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}}{t_{GeSi}^2(1 + \frac{\varepsilon_{GeSi}t_{Si}}{\varepsilon_{Si}t_{GeSi}})},$$

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$$\alpha = \frac{a_2 a_3 - a_1 a_4}{a_1 - a_4}, \beta = \frac{c_2 a_2 - c_1 a_4}{a_1 - a_4}$$

$$a_1 = \frac{2 + \frac{2\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox}} + \frac{\varepsilon_{ox} t_{GeSi}}{\varepsilon_{GeSi} t_{ox}}}{t_{Si}^2 (1 + \frac{\varepsilon_{Si} t_{GeSi}}{\varepsilon_{GeSi} t_{Si}})}, a_2 = \frac{2}{t_{Si}^2 (1 + \frac{\varepsilon_{Si} t_{GeSi}}{\varepsilon_{GeSi} t_{Si}})},$$

$$a_3 = \frac{2 + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox}}}{t_{GeSi}^2 (1 + \frac{\varepsilon_{GeSi} t_{Si}}{\varepsilon_{Si} t_{GeSi}})}, a_4 = \frac{2}{t_{GeSi}^2 (1 + \frac{\varepsilon_{GeSi} t_{Si}}{\varepsilon_{Si} t_{GeSi}})}$$

$$c_1 = \frac{qN_A}{\varepsilon_{Si}} - \frac{2\frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox}} + \frac{\varepsilon_{ox} t_{GeSi}}{\varepsilon_{GeSi} t_{ox}}}{t_{Si}^2 (1 + \frac{\varepsilon_{Si} t_{GeSi}}{\varepsilon_{GeSi} t_{Si}})} V_G',$$

$$c_2 = \frac{qN_A}{\varepsilon_{GeSi}} - \frac{\frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox}}}{t_{GeSi}^2 (1 + \frac{\varepsilon_{GeSi} t_{Si}}{\varepsilon_{Si} t_{GeSi}})} V_G'$$

$$V_G' = V_G + \Delta\varphi_{MI}$$

IV. SIMULATION OF VOLTAGE MODEL

To verify the accuracy of the threshold voltage model, we use Matlab for numerical analysis and use ISE to simulate the model proposed in the previous section.

The parameters used are as following: Work function of gate material $\Delta\varphi_{MI}$= 4.6eV, T=300K, Drain bias $V_D = 0$, the source/drain/intrinsic doping $N_s = N_d = 10^{20}cm^{-3}$, $N_A = 2\times 10^{20}cm^{-3}$. The results are presented as the following figures.

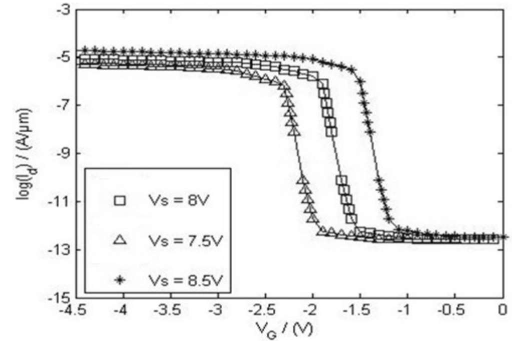

Figure 2. Transfer characteristic curve of Hetero P-IMOS

Fig. 2 presents the transfer characteristic curve of Hetero P-IMOS under different source voltage, including $L_G = L_{in}$ = 100 nm. We can easily spot the influence of the source voltage on the threshold voltage. When V_S reduces, the device needs the higher $|V_G|$ so as to attain the critical point of the avalanche breakdown.

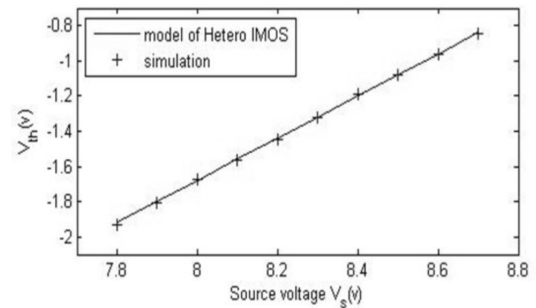

Figure 3. Variation of threshold voltage with Source voltage

Fig.3 shows the variation of threshold voltage with Source voltage. It can be found that simulation results and calculated results of model agree very well with each other. We can observe that $|V_{th}|$ increases when V_S decreases.

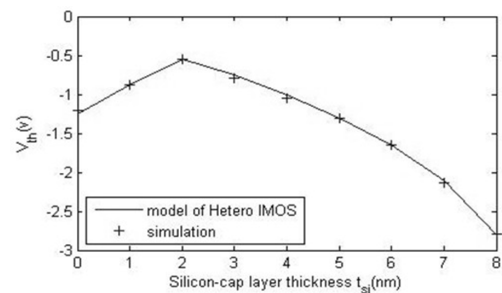

Figure 4. Variation of threshold voltage with t_{si}

Threshold voltage (V_{th}) as a function of the silicon-cap layer thicknesses is shown in Fig.4. By increasing t_{si}, the electric field in the buried channel is decreased. Thus the ionization rate decreases and avalanche breakdown occurs at higher gate voltages. As a result, V_{th} increases. An optimum

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silicon-cap layer thickness equal to 2 nm is obtained for the structure.

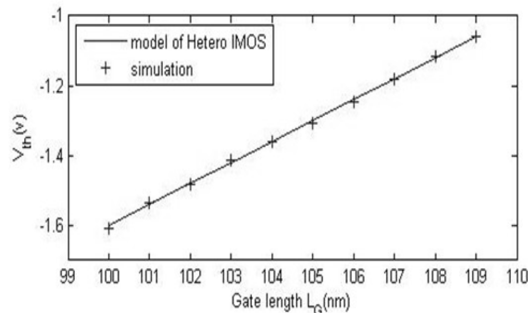

Figure 5. Variation of threshold voltage with the gate length

From Fig.5 we can see that for a given polarization Vs = 7.8V, the threshold voltage $|V_{th}|$ is smaller for higher L_G/L_{in} ratios. However, the higher L_G/L_{in} is, the higher subthreshold slope is. Besides, with a higher L_G/L_{in}, a bigger part of channel is controlled by the gate. Thus, the ionization rate and avalanche breakdown occurs at a smaller $|V_{th}|$.

V. CONCLUSION

A threshold voltage model of Hetero IMOS is proposed in this paper. The results of the model are in good agreement with that of simulation. The model in the paper can be easily used for the analysis and design of IMOS so that it is utilized to VILS design..

REFERENCES

[1] Choi W Y, Choi B Y, Woo D S, Lee J D, Park B G, "Reverse-order source/drain formation with double offset spacer (RODOS) for low-power and high-speed application", 2003 IEEE Trans. Nanotechnol 2 210

[2] Zheng X H, Huang A P, Yang Z C, Xiao Z S, Wang M, Cheng G A, "Diffusion behavior of dual capping layers in TiN/LaN/AlN/HfSiOx/Si stack", 2011 Acta Phys. Sin. 60 017702 (in Chinese)

[3] K. Gopalakrishnan, P. B. Gri_n, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q", IEDM, 2002. pp. 289-292.

[4] F. Mayer, C. Le Royer, G. Le Carval, L. Clavelier, and S. Deleonibus, "Static and Dynamic TCAD Analysis of IMOS Performance: From the Single Device to the Circuit," IEEE Trans. Electron Devices, vol. 53, no. 8, pp. 1852-1857, Aug. 2006.

[5] K. Gopalakrishnan, "Impact-Ionization MOS and its Derivatives for Logic and Memory", Thesis, 2004.

[6] K. Gopalakrishnan, R. Woo, C. Jungemann, P. B. Griffin, and J. D. Plummer, "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit simulations, Trans. Electron Devices", pp. 69-76, Jan. 2005.

[7] Hamed Nematian, "Reducing Breakdown Voltages in Impact Ionization Metal-Oxide-Semiconductor (I-MOS) Devices Using Hetero Structure", IEEE. 2008. pp.114-117.

[8] Li Yu-Chen, Zhang He-Ming "A analytic model for the threshold-voltage of novel high-speed semiconductor device IMOS", Acta Phys. Sin. 2012. Vol. 61, No. 4, pp1-5.

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