Low-Power Near-threshold MOS Current Mode Logic with Power-Gating Techniques

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***Abstract*—MOS Current-Mode Logic (MCML) is usually used for high-speed applications. However, the large static power dissipation of MCML circuit limits its application in portable devices. In this work, we proposed a power-gating (PG) technique to reduce the standby power of the near-threshold MCML. The PG 1-bit full adder and a mod-10 counter are designed and simulated using HSPICE at 45nm CMOS technology with predictive technology model (PTM) model. The simulation results show that the standby power of the PG-adder and PG-counter is only 1.0nW and 3.0 nW, respectively. And the performance of the PG MCML circuits does not deteriorate.**

Keywords-lowe power; power-gating; current mode logic; near-threshold

I. INTRODUCTION

MOS Current-Mode Logic (MCML) is one of the most widely used logic styles in high-speed circuits such as high-speed processors and Gbps multiplexers for optical transceivers, due to its lower logic swing [1-3]. Meanwhile, because of its low switching noise, MCML is adapted in the mixed signal ICs to avoid the degradation of resolution. Recently, MCML has obtained some attentions in cryptographic circuits design due to its robust of the power analysis attacks [4].

However, the large static power consumption of MCML, due to its constant operation current, limits the range of applications. Hence, the low power MCML logic design has obtained quit some attentions [5-8]. P. Heydari and G. Caruso presented the methodologies for the low-power design of MCML-based ring oscillators and buffer chain, respectively. Mohab H. Anis et al. proposed the multi-threshold MCML (MTMCML) technology that allows the reduction of the minimum supply voltage of the two-level MCML circuits, hence lower the power dissipation of the MCML circuits [8].

To reduce the static power, several power-gating techniques for MCML circuits are proposed [4，9]. The proposed methods use a sleep-transistor inserted in series with the supply voltage or current source to reduce the standby power. While, for near-threshold MCML which using the minimum supply voltage, the inserted sleep-transistor will affect the operation voltage of the MCML circuits, and then change the state of the transistors. Therefore, a new low static power design method should be investigated for near-threshold MCML circuits.

In this paper, we present a power-gating near-threshold MCML circuits which use a transistor to pull down the bias voltage of the current source transistor to ground during the sleep mode, to reduce the static power. This paper is organized as follows. In section 2, the conventional MCML circuits are described, and the minimum operating voltage of the MCML is analyzed. In section 3, the power-gating technique of near-threshold MCML is introduced. Taken as examples, the power-gating 1-bit full adder and a mod-10 counter are realized and simulated by HSPICE at 45nm CMOS process with PTM model in section 4 [10]. The conclusion is dedicated at last.

II. REVIEW OF MCML CIRCUITS

A. The Conventional MCML Circuits

The basic MCML inverter/buffer and its bias circuit are shown in Figure 1. The MCML inverter is composed of three main parts: the load transistors P1 and P2, the full differential pull down switch network consisting of N1 and N2, and the current source transistor Ns. The load transistors are designed to operate at linear region with the auxiliary of the control voltage *VRFP* produced by the bias circuit, which also controls the output logic swings [3]. The pull-down network (PDN) NMOS N1 and N2 are used to perform logic operation. The NMOS Ns is used to provide the constant current source, which is mirrored from the current source in the bias circuit.

The operation of MCML is performed in the current domain. The pull down network switches the constant current between two branches, and then the load converts the current to output voltage swings. The high and low digital logic levels are $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - I_B R_D$, respectively, where R_D is the PMOS load resistance. The logic swing is $\Delta V = V_{OH} - V_{OL} = I_B R_D$.

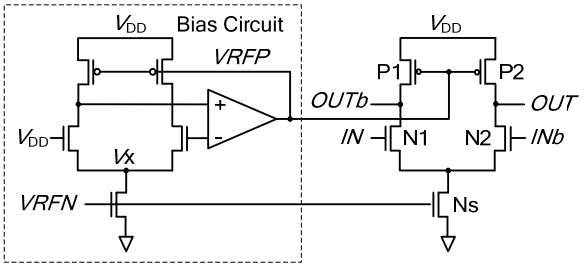

Figure 1. MCML inverter/buffer and its bias circuit.

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Figure 2 shows the MCML universal logic gate, XOR2/XNOR2, 2-1MUX and D-Latch. The MCML universal logic gate can realize any of the basic two-input logic functions, namely, the AND2, NAND2, OR2, and NOR2 operations.

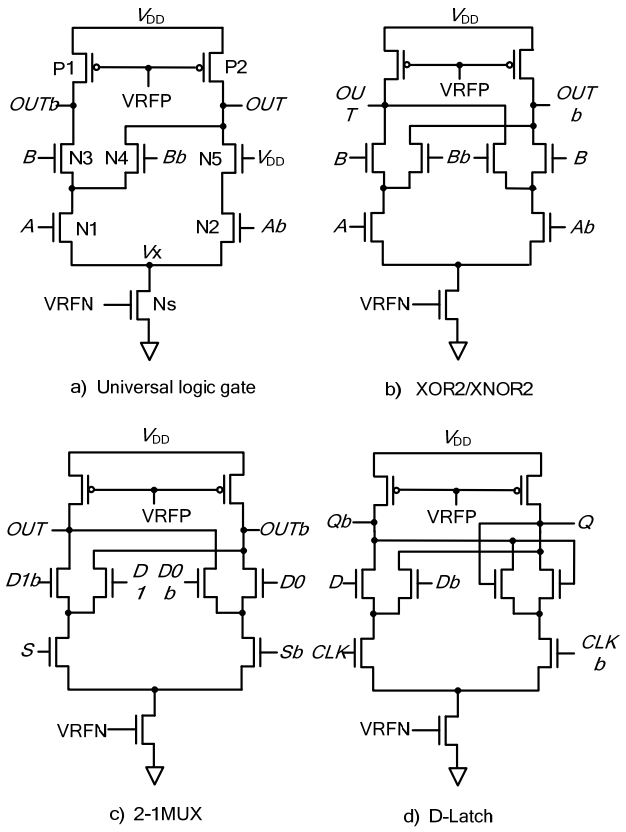

Figure 2. The basic MCML Gates, a) Universal logic gate, b) XOR2/XNOR2, c) 2-1 MUX , d) D-Latch.

The optimization performance metrics of the MCML gate mainly include propagation delay, power dissipation and power-delay product. The delay time of a MCML gate can be calculated assuming that, at each transition, the whole I_B, ideally, flows through one branch of the differential pair and charges the total load capacitance C, is given by

$$t_d = 0.69RC = 0.69C(\Delta V / I_B), \quad (1)$$

The power consumption of a MCML gate is independent of the switching frequency, and it is given by

$$P = V_{DD} \times I_B, \quad (2)$$

where V_{DD} is the supply voltage. I_B is the bias current of the MCML gate.

Finally, the power-delay product is independent of the switching frequency and can be calculated as

$$PDP = P \times t_d = 0.69 V_{DD} \times \Delta V \times C, \quad (3)$$

B. Near-threshold MCML Circuits

Recently, the near-threshold computing is presented [11, 12]. The supply voltage of near-threshold circuits is slightly above the threshold voltage of the transistors. This region obtains much of the energy savings and more favorable performance, so as to the MCML circuits.

As shown in (2), power dissipation in MCML is equal to $V_{DD} \times I_B$. So the power dissipation of MCML can be saved by reducing either the V_{DD} or the I_B. While I_B can not be reduced under a certain limit, otherwise performance will be degraded. Hence, reducing the supply voltage is an effective method to lower the power consumption of MCML circuits. According to (1-2), it can be seen that reducing the supply voltage of MCML wouldn't degraded the performance of MCML. Meanwhile, the power-delay product can also be improved as the V_{DD} decreased.

In order to get the most efficient point of the near-threshold MCML circuit, the minimum supply voltage should be estimated. The minimum operating supply voltage for an MCML circuit is defined as the lowest voltage at which the differential pairs as well as the current source are made to operate in the saturation region to ensure correct functionality and adequate performance[12]. The V_{min} of MCML universal logic gate, shown in Figure 2, can be expressed as

$$V_{min} = V_{ds1,sat} + V_{dss,sat} + V_{gs3}, \quad (4)$$

where $V_{ds1,sat}$, $V_{dss,sat}$ and V_{gs3} are the drain-source saturation voltage for N1, drain-source saturation voltage for Ns and the gate-source voltage for N3 respectively. Then, the V_{min} of MCML universal logic gate is

$$\begin{aligned} V_{min} = & \frac{I}{2W_1 C_{OX} v_{sat}} \left(\sqrt{1 + \frac{4E_{sat} W_1 L_1 C_{OX} v_{sat}}{I}} - 1 \right) \\ & + \frac{I}{2W_s C_{OX} v_{sat}} \left(\sqrt{1 + \frac{4E_{sat} W_s L_s C_{OX} v_{sat}}{I}} - 1 \right) \\ & + V_{th3} + \frac{I}{2W_3 C_{OX} v_{sat}} \left(1 + \sqrt{1 + \frac{4E_{sat} W_3 L_3 C_{OX} v_{sat}}{I}} \right) \end{aligned}, \quad (5)$$

where E_{sat}, C_{ox} and v_{sat} are the saturation electric field, oxide capacitance, and saturation velocity, respectively, while W and L are the transistor effective width and length, respectively.

According to the (5), the minimum operating voltage of the MCML can be estimated. At the 45nm CMOS process using the NCSU PTM model, the minimum operation voltage of the MCML gate is about 0.7V according to the (5).

III. POWER-GATING NEAR-THRESHOLD MCML CIRCUITS

Power gating is a circuit design technique which reduces the static power consumption of a digital circuit by inserting power switches in the supply path, and has been most widely used in industrial products. There are two implemented schemes of power gating technique: coarse-grain power gating, in which complete blocks are disconnected from the power supply and the ground through a common power switch, and fine-grain power gating, in which every standard cell contains a sleep transistor internally.

Different power gating topologies for MCML circuits are depicted in Figure 3. The solutions (a) and (b) use a transistor to pull down the bias voltage VRFN to ground during the sleep mode. Solution (c) applies just a ON signal to the gate of the current source and connects the bulk voltage to the bias voltage *VRFN*. Options (d) and (e) consist of an additional sleep transistor in series with the current source and V_{dd}, respectively.

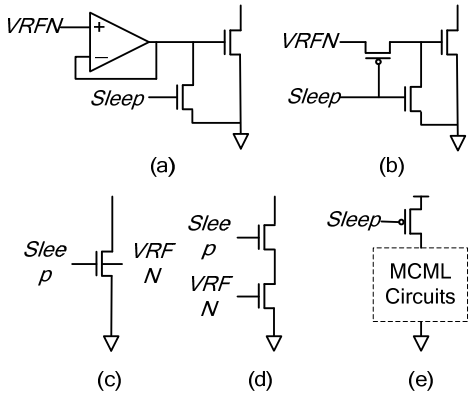

Figure 3. Different power gating techniques for MCML circuits.

Solution (a) was discarded since it uses a follower amplifier which leads to a significant area overhead. With 500mV to 1 V voltage to modulate the bias current, solution (c) is difficult to be implemented in practice. Option (d) and (e) are not suite the near-threshold circuits because the additional sleep transistors will further decease the operation voltage. For all the above reasons, we selected solution (b) to implement the power-gating near-threshold MCML circuits. The proposed scheme of power-gating near-threshold MCML circuits is shown in Figure 4.

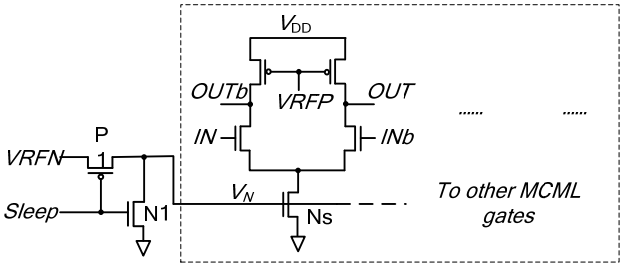

Figure 4. The proposed scheme of power-gating MCML circuits.

The proposed technology has two operating modes, the active mode and the sleep mode. In the active mode, the sleep transistor P1 is turn on and N1is turn off because *Sleep* is set to 0. Therefore, the gate of the current source transistor is connected to the *VRFN* to execute the normal operation. In the sleep mode, *Sleep* is set to 1, then the sleep transistor P1 is turn off, and N1 is turn on. Therefore, the current source is turn off, which reduces the power consumption by the standby current in the sleep mode.

IV. SIMULATION RESULTS

In the section, a power-gating near-threshold MCML 1-bit full adder and a mode-10 counter are designed to demonstrating the low power feature of the proposed technology.

The proposed circuits are simulated with HSPICE at 45nm CMOS technology. The supply voltage is 0.7V and the bias current is 10uA. In order to simulate the work environment of the MCML logic circuits, the testing platforms are shown in Figure 5. In order to assure the fairness of the comparison, each input is driven by buffered signals and each output is loaded with buffers, which provide a realistic simulation environment reflecting the operation in actual applications.

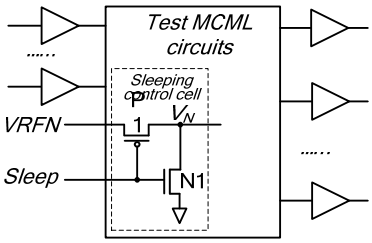

Figure 5. Test platform.

A. Power-gating(PG) MCML Full Adder

The conventional 1-bit full adder circuit is shown in Figure 6. The PG MCML full adder is simulated using HSPICE at the 45nm CMOS process using the NCSU PTM model. The device size of PMOS load transistors and current source NMOS transistor is taken with W/L =4λ/2λ and 20λ/6λ, respectively. The device size of NMOS transistors of the differential pair is taken with 8λ/2λ, and λ=25nm. The V_{th0} of the NMOS transistors is 0.466V.

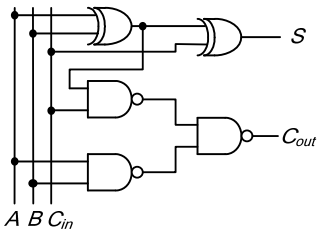

Figure 6. Power-gating MCML 1-bit full adder.

For comparison, the conventional MCML full adders are also verified using the 45nm CMOS process based on the same architecture. The standby power, propagation delay of the PG and conventional full adders is shown in TABLE I.

TABLE I. POWER DELAY COMPARITION OF THE ADDERS

	Active Power (μW)	***Standby power*** (μW)	***Average Propagation Delay***(ps)
Conventional Adder	32.9	——	37.7
PG Adder	32.9	0.001	37.8

The simulation results show that the active power of the tow adders is 32.9 μW. The standby power of the PG-adder is only 0.001 μW. The average delay of PG-adder is nearly equal to the conventional one.

B. The Power-Gating(PG) Mod-10 Counter

The mod-10 counter, shown in Figure 8, is implemented with *DFF*s and other combinational gates as shown in the Figure 2. The bias voltage of the current sources of all the cells in the counter is the controlled by the sleeping control cell. The *DFF* is composed of two D-latch as shown in Figure 7.

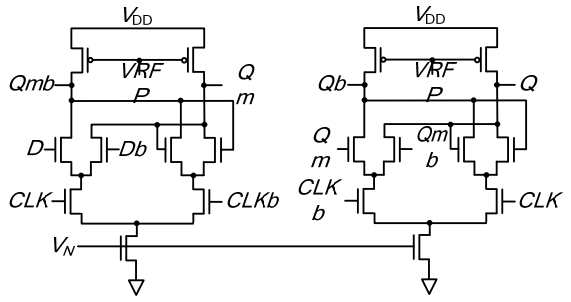

Figure 7. Master-Slave PG MCML *D*-Flipflop.

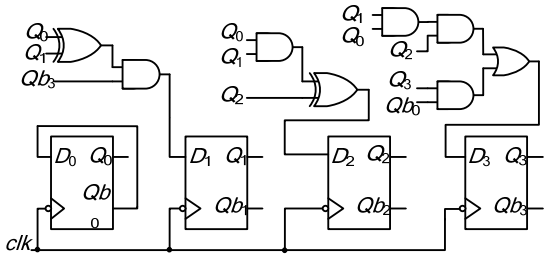

Figure 8. Schematic view of a PG mod-10 counter.

The proposed PG-counter and conventional counter are simulated through HSPICE with the 45 nm PTM CMOS technology with a supply voltage of 0.7V. In the normal mode, the power consumption of the PG-counter is 104.8μW equal to the conventional counter circuit. And, in the sleep mode, the standby power consumption of the PG counter is only 0.003 uW. Hence, the proposed power-gating technique is an effective method to reduce the standby power of the MCML circuits.

V. CONCLUTIONS

The standby power of the MCML circuits is the main drawback for its widely using for many portable applications. The active power consumption of MCML circuits can be reduced by the near-threshold computing technology, while the standby power is still large. In this paper, we present a power-gating technology to reduce the standby power of the MCML circuits. The proposed technology using a sleeping control cell to control the gate bias voltage of the current source to implement the two operation mode: sleeping mode and active mode. A power-gating adder and mod-10 counter are designed and simulated to verify the validation and effectiveness. The HSPICE simulation results show that larger standby power consumption saving can be achieved and the performance is almost not affected.

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