A High DC Gain Op-Amp for Sample and Hold Circuits

Biao Li
Electronic Engineering College
Chengdu University of Information Technology
Chengdu
dabiao.lee@gmail.com

***Abstract*— Being a core component of an analog-to-digital converter (ADC), the operational amplifier is expected to provide sufficient DC gain and bandwidth to make the output amplitude less than ½ Least Significant Bit (LSB) in a half clock cycle. However, due to the limitation of the operational amplifiers in DC gain and bandwidth, most ADC is limited to 10-Bit, 100 Million Samples per Second (MSPS) [1-3]. This paper designs a gain-boosted operational amplifier in a 0.18um CMOS technology with a 1.8V supply. It is shown that the proposed amplifier achieves 89.8dB gain and 2.63GHz unity-gain frequency, greatly outperforming competing techniques. In addition, the proposed amplifier supports 12-Bit resolution. Compared to other amplifiers with similar architecture, this one has a lower cost.**

Keywords-operational amplifier, DC gain, unity-gain bandwidth, ADC, CMFB

I. INTRODUCTION

As the core component in an analog circuit, the operational amplifier, which has a crucial role in the circuit performance and can become the main bottleneck. On the other hand, the demand for amplifiers with high DC gain and bandwidth is increasing. In a high speed and high resolution ADC, operational amplifiers are expected to have both high DC gain and high unity-gain frequency in order to satisfy the accuracy and fast setting requirements of the system.

However, the DC gain and the unity-gain bandwidth are two contradictory demands. High DC gain can be achieved using long-channel devices and multistage design. But in order to achieve high unity-gain bandwidth, a single-stage design with short channel devices is usually required [4]. Practically, the DC gain of a traditional fold-cascade operational amplifier is limited to 75dB [5]. Although the two-stage operational amplifier [6, 7] can further improve the DC gain and output voltage swing, the speed of the operational amplifier will be degraded [8]. So it is very difficult to achieve both high DC gain and high unity-gain bandwidth for high resolution and high speed ADC.

On the other hand, although there are already operational amplifiers having both high DC gain and high bandwidth performance, the extraordinary cost seriously impedes their popularity in commercial market. Therefore, it is of great interest to develop amplifiers with both high DC gain and bandwidth performance at a low cost.

In this paper, we propose a gain-boosted operational amplifier in a 0.18um CMOS technology with a 1.8V supply. The simulated results show that the operational amplifier achieves 89.8 dB DC gain and a unity-frequency of 2.63GHz. The performance is much better than most amplifiers in terms of both DC gain and bandwidth. The proposed amplifier is very suitable for a sample and hold circuit in a 12-Bit 500MSPS pipeline ADC. Moreover, the cost of the proposed amplifier is much lower than those amplifiers with similar performance.

The rest of the paper is organized as follows. Section 2 describes in detail the proposed gain boosted folded cascade amplifier. The simulated results are presented and discussed in Section 3. Finally, Section 4 concludes the paper.

II. PROPOSED DESIGN OF GAIN BOOSTED CASCADE AMPLIFIER

In high resolution and speed ADC, the operational amplifier is mostly designed with BiCMOS technology, which is much more expensive than CMOS technology.The proposed amplifier is designed by CMOS technology which includes two amplifiers: the main amplifier and two additional folded-cascade amplifiers named as amp1 and amp2, as shown in Figure 1. The amp1 uses NMOS transistors as the input stage, while the amp2 uses PMOS as the input. In this system, the output impendance of the main amplifier is increased by the gain of the additional amplifiers amp1and amp2. The gain of the total amplifier is given by

$$A_v = g_{m1} \cdot \{[g_{m5} r_{o5} \cdot (r_{o3} \| r_{o1})(1 + A_{v,amp1})] \| [g_{m7} r_{o7} \cdot r_{o9}(1 + A_{v,amp2})]\} \quad (1)$$

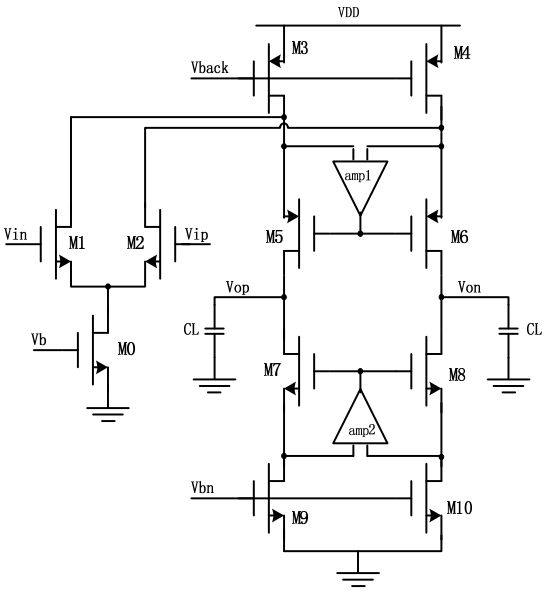

Figure 1 The gain-boosted folded-cascade amplifier

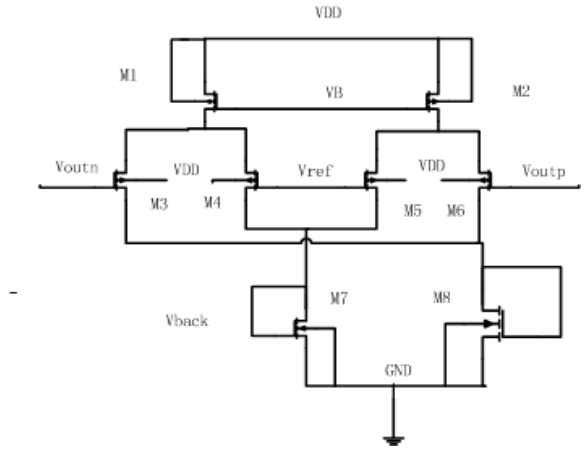

Figure 2 The common-mode feedback (CMFB) circuit of amp1

where g_{m1} g_{m5} g_{m7} are the transconductances of the M_1 , M_5 , M_7 , r_{o1} r_{o3} r_{o5} r_{o7} r_{o9} are the small equivalent output resistance of M_1 , M_3 , M_5 , M_7 , M_9 and the $A_{v,amp1}$ $A_{v,amp2}$ are the DC gains of the additional gain stage of amp_1 , amp_2 .

In the structure of the gain-boosted operational amplifier, there are two potential serious problems for the time-domain performance, i.e. doublet and instability. Doublet which can slow the setting performance of the amplifier is caused by the poles of the auxiliary amplifier, and exists around the unity-gain bandwidth of amp1.Pushing up the doublet to a higher frequency is a common solution. However, if the doublet is very close to the non-dominant pole of the main operational amplifier, the stability becomes degraded, due to the existence of amp1 which constructs a closed-loop with M5 and M6. The reason for this is that there are two poles in the loop. One is located at the output of the additional amplifier amp1 and the other at the source of the transistor M5. The second is equal to the non-dominant pole of the main amplifier. The common solution is to use a compensation capacitor to set the unity-gain frequency of the additional amplifier between the non-dominant pole and the unity-gain frequency of main amplifier. However, the method of using a compensation capacitor is very complicated and usually empirically implemented.

In this paper a simple but more accurate scheme is proposed. After finishing the main operational amplifier, the parasitic capacitance is mathematically calculated from the gate of M5 to ground. When a closed-loop is generated by the additional amplifier amp1 with M5, when according to the parasitic capacitance , the load capacitance can be calculated as

$$CL \approx Cbg+(1+A)Cgd+(1+A1)Cgs \quad (2)$$

Where Cgs is the parasitic capacitance from the gate to the source M5, Cgd from the gate to the drain of M5,and Cbg from the gate of M5 to the body .A is the DC gain from the drain to the gate of M5 and A1 is the DC gain from the source to the gate of M5 which is approximately equal 1. During the design of the additional amplifier amp1, the value of the load capacitance is set equal to C_L . In addition, the unity-gain frequency is defined within the safe range. Without the need for the compensation capacitor, the instability and the slow setting problems can be effectively avoided.

It is worth to point out that in the proposed main amplifier, the common-mode feedback block(CMFB)adopts switched capacitance structures. As a component of the amplifier, the CMFB is of great importance to the performance of the proposed amplifier. Since the capacitance is also set as the load capacitance of the proposed operational amplifier. With too large capacitance, the unity-gain bandwidth can be pushed down. Otherwise, if the capacitance is too small, the accuracy of the voltage that return to the amplifier can be degraded by the charge injection of switches. Moreover, the CMFB in the proposed system allows a larger output swing. Consequently, energy savings can be further expected compared to a continuous time CMFB circuit.

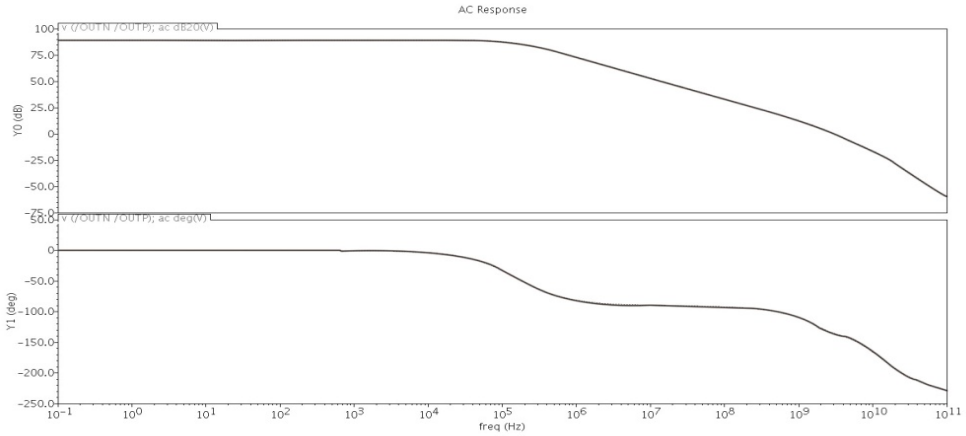

Figure 3 The diagram of the AC analysis

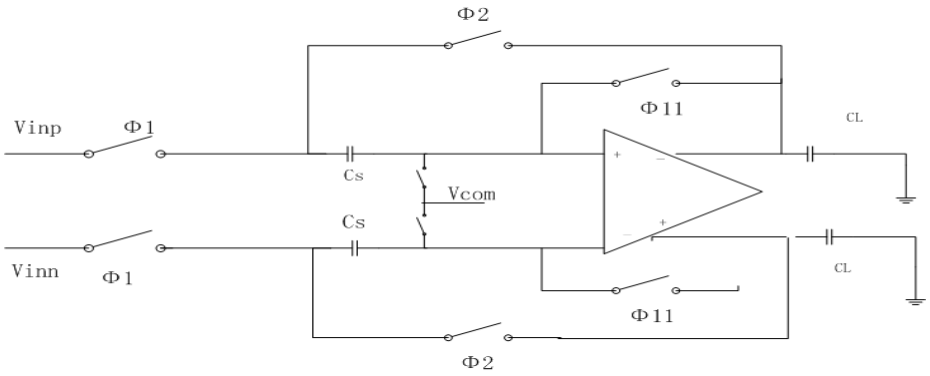

Figure 4 Sample and hold circuit

Since the output of each additional amplifier does not need a large swing, a continuous time CMFB circuit is used in amp1 and amp2. Figure 2 presents the CMFB structure of amp1 as an example.

III SIMULATION RESULTS AND DISCUSSION

The gain-boosted op-amp has been performed in a 0.18um CMOS technology with a 1.8V supply and 4.8pF load capacitance. The AC simulated results are given in Figure 3. According to the simulation results, a DC gain of 89.8dB, a unity-gain bandwidth of 2.63GHz and a phase 55 phase margin is achieved.

In addition, the transient behavior has been simulated by placing the gain-boosted amplifier in a sample and hold circuit to provide a global feedback with β=1 and Cs=CL=1.2pF as shown in Figure 4. For a sample and hold circuit in a 12-Bit 500MSPS pipeline ADC, the Verror1 caused by the limited DC gain of the amplifier should be less than 1/2LSB, according to the equation

$$Verror1 = (1/A\beta)\,Vin, \quad LSB = Vin/2N \tag{3}$$

where N is the bits of resolution of the ADC and Vin is the full input voltage 1V. According to that the DC gain is specified to be more than 72dB. The error Verror2 raised by the limited bandwidth of the amplifier should not exceed 1/4LSB as

$$Verror = -e^{\frac{-t}{\tau}} V_{in} < \frac{1}{4} LSB \tag{4}$$

and τis a time constant parameter as

$$\tau = \frac{1}{\omega_{-3db}} = \frac{1}{2\pi f_u \beta} \tag{5}$$

where $t = \frac{3}{8f_{sample}}$, f_{sample} = 500MSPS, ω_{-3db} is the -3dB frequency of the closed-loop amplifier and f_{sample} is the sample rate. So the unity-gain bandwidth of the amplifier is theoretically 2.06GHz.

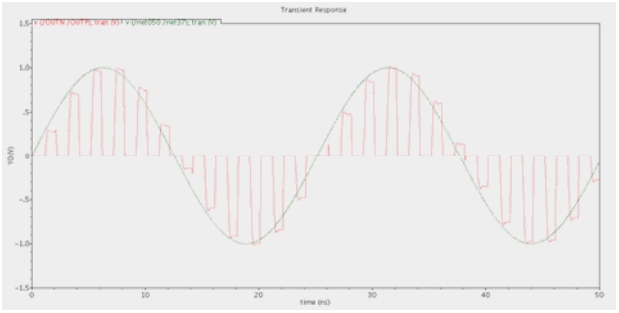

Figure5 Transient analysis of the sample and hold circuit

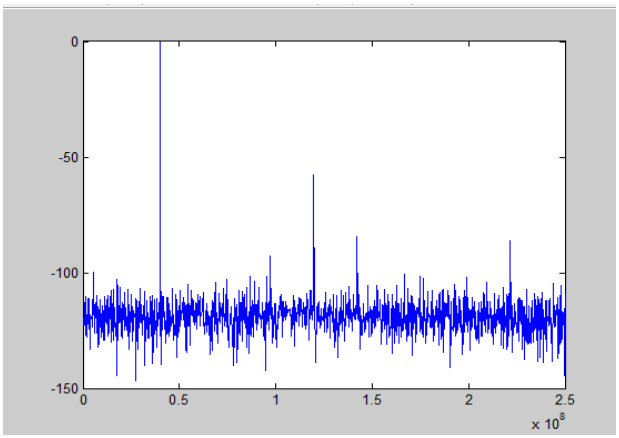

Figure 6 DFT spectrum of the output signal

If the DC gain and the unity-gain bandwidth is lower than the calculate value, the operational amplifier cannot be qualified for the 12Bit 500MSPS pipeline ADC.

The transient simulation results of the sample and hold circuit are illustrated in Figure 5. Figure 6 shows the DFT plot of the output signal with input frequency =39.7949MHz, fs=500MHz, where fs is the sample rate.

The simulation results show that the setting time for 0.01% accuracy is 0.95ns in the proposed system. However, in related literature [9, 10] the unity-gain bandwidth is only 822MHz and 807MHz. The setting time for 0.048% accuracy is 3.5ns in [9] and 9.7ns in [10]. So the proposed amplifier significantly outperforms the references. In addition, the Spurious Free Dynamic Range(SFDR) is reported as 57.59dB and the Signal-to-Noise ration (SNR) is 83.72dB. According to the above results, the proposed amplifier is able to support 13.6 Effective Number of Bit(ENOB) and a sample rate of 500MSPS..

IV CONCLUSIONS

In this paper, a gain-boosted operational amplifier with both high DC gain and unity-gain bandwidth is proposed. The proposed amplifier is implemented in 0.18um CMOS with a 1.8V supply. The simulation results demonstrate that the proposed amplifier achieves 89.8dB DC gain and 2.63GHz unity-gain bandwidth with a 4.8PF load capacitance. The transient simulation shows the amplifier is suitable for a 12-Bit 500MSPS Pipeline ADC.

REFERENCES

[1] Yang Zhanpeng and Ye Xingnig, “12 bit 10MS/s Pipelined Analog-to-Digitial Converters' IC Design and Application,” 2011.01.015

[2] CHEN Mei-na, DAI Qing-yuan, ZHU Hong-wei and JIANG Shen-fei, “A Sample/Hold circuit for 10-Bit 100MS/s Pipelined A/D converters,” Microelectronics, Feb.2007.

[3] J.Doernberg, P.R.Gray, and D.A.Hodges,”A 10-bit 5-Msamples/s CMOS Two-Step Flash ADC,” IEEE J. Solid-State Circuits,Vol.24,No.2.pp.241-249,Apr 1990.

[4] Gulati, K., and Lee, H.-S, “A high-swing CMOS telescopic operational amplifier,” IEEE J. Solid-State Circuits, 1998, 33, (12), pp. 2010–2019

[5] Wang Shaoqing, Xu Ken and Feng Yongjian, “A Fully Differential Fold-Cascode CMOS Operational Amplifier,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol.41, no.3, pp.241-243, Mar 1994.

[6] Zou Rui，Ze Dedong and Hong Zhiliang, “Optimal Design of CMOS Fully Differential Two Stage OTA,” Journal of Computer—Aided Design&Computer Raphics，VOI．I7．NO．9 Sep.，2005

[7] Zhu Zhen，and Wang Tao, “A Full Differential，Low Power Consumption CMOS Operational Transconductance Amplifier（OTA),”, 2000.

[8] Razavi,”Design of analog CMOS integrated circuits,” McGraw-Hill Companies 2000.

[9] SU Li and Qiu YuLin, “Design of a Fully Differential Gain-Boosted Folded-Cascode Op Amp with Setting Performance Optimization,” IEEE conference on Electron Devices and Solid-State Circuits, pp441-444, 2005.

[10] D. Shahrjerdi, B. Hekmatshoar, M. Talaie and O. Shoaci, “A Fast Setting, High DC Gain,Low Power OPAMP Design for High Resolution, High Speed A/D onverters,” ICME, Cairo, Egypt, Dec.9-11, 2003.