

An application of LDPC code for wireless coherent-light commutation in atmospheric channel

Ning Hao^{*a}, Yang'an Zhang^a, Jinnan Zhang^a, Minglun Zhang^a, Xueguang Yuan^a

^aState Key Laboratory of Information Photonics and Optical Communications of Beijing University of Posts and Telecommunications. P.O. Box 66 (BUPT)
Beijing, China 100876 ,Tel: 86-10-61198081
e-mail: haoning212@126.com

Abstract—Low Density Parity Check code is more and more taken seriously in high-speed transmission. In this article we represent a LDPC coder and decoder which based on IEEE802.16e and realize the coder and decoder with Virtex-5 FPGA. By using Matlab to make an off-line system simulation, we analyzed and compared the LDPC performance under the different length of code for LDPC code then analyzed the influence of different iteration to the LDPC BER performance of decoder.

Keywords—Low Density Parity Check code(LDPC) , IEEE802.16e, Bit-Flipping algorithm (BF), parity check matrix

I. INTRODUCTION

LDPC is short for Low Density Parity Check codes which presented by Gallager at 1960s. This code is a kind of liner block code that based on parity check matrix. In the code there are a little non-zero elements and much more zero so is named. But the advantage of LDPC was ignored for a long time, for the reason that there were no effective methods to calculate in 1960s and also the Concatenated code was regarded as a better performance in coder at that time. While in 1996, Mac Kay found that the performance of LDPC has the ability of exceeding the Turbo code, so it became famous again and the researching of LDPC steps into a new period. Reports of the researching about LDPC indicate that performance of LDPC could approach to the Shanno limit in the last few years. In BIAWGN there is only 0.00d5dB difference from Shannon limit by using 1/2 code rate LDPC.

Bipartite graph could be used to indicate the LDPC, which is made up by Variable Nodes, Check Nodes and the Edges that between them. Variable Nodes indicate the information bit, so as to a column of parity check matrix. Check Nodes indicate the check sequence, so as to a row of parity check matrix. Then the Edges connect the Variables and Check Nodes, which indicate the non-zero elements in the parity check matrix. In bipartite graph, if a path from one node could loopback to itself is called ring. It is very harmful appearance when to decode a sequence which has a lot short rings in it. So it is better that avoiding rings when coding the sequence.

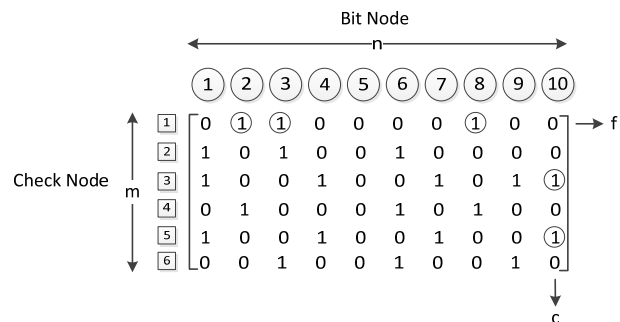


Figure 1. Regular Check matrix.

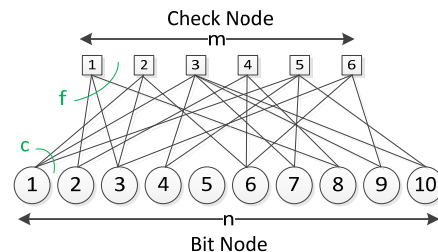


Figure 2. Tanner Graph.

In this experiment a million gates FPGA of Xilinx Virtex-5 is used to realize the LDPC coder and LDPC decoder, the system block graph shown as below,

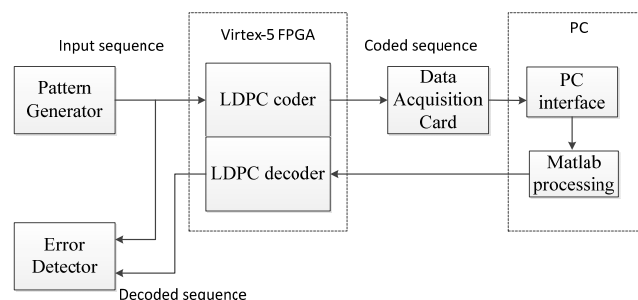


Figure 3. System testing block diagram.

II. SYSTEM SETUP

A. Coder of LDPC module

For efficient encoding of LDPC, H are divided into the form

$$H = \begin{bmatrix} A & B & T \\ C & D & E \end{bmatrix}$$

Where A is $(m-z) \times k\alpha$, B is $(m-z) \times z$, T is $(m-z) \times (m-z)$, C is $z \times k$, D is $z \times z$, and finally E is $z \times (m-z)$. $\begin{pmatrix} B \\ D \end{pmatrix}$ and D correspond to the expanded $\vec{h}_b$ and $\vec{h}_b(m_b - 1)$, respectively.

Let $v = (u, p_1, p_2)$ where u denotes the systematic part, p_1 and p_2 combined denote the parity part, p_1 has length z , and p_2 has length $(m-z)$. The definition equation $(H \cdot v^T) = 0$ splits into two equations, as in Equation (A.2) and Equation (A.3).

$$Au^T + Bp_1^T + Tp_2^T = 0 \quad (A.1)$$

and

$$(ET^{-1}A + C)u^T + (ET^{-1}B + D)p_1^T = 0 \quad (A.2)$$

Define $\phi = (ET^{-1}B + D)$ and with the parity check matrix as indicated $\phi = I$. Then from Equation (A.2), it can be concluded that

$$p_1^T = (ET^{-1}A + C)u^T \quad (A.3)$$

and

$$p_2^T = T^{-1}(Au^T + Bp_1^T) \quad (A.4)$$

As a result, the encoding procedures and the corresponding operation can be summarized below and illustrated in Figure 4,

- (1) Compute Au^T and Cu^T .
- (2) Compute $ET^{-1}(Au^T)$.
- (3) Compute p_1^T by $p_1^T = ET^{-1}(Au^T) + Cu^T$.
- (4) Compute p_2^T by $TP_2^T = Au^T + Bp_1^T$

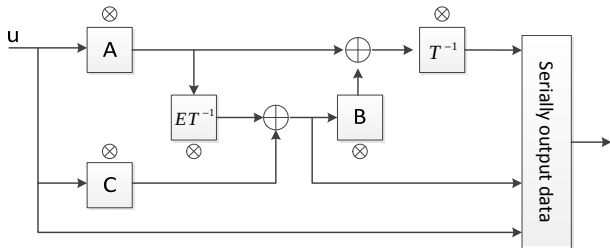


Figure 4. Block diagram of LDPC coder algorithm

B. Decoder of LDPC module

Bit-Flipping, BF algorithm is a kind of hard decision decoding algorithm especially for LDPC which firstly

proposed by Gallager. It is very easy to be realized on hardware and it has a very simple structure, because in the process of decoding only to handle the bit 0 and bit 1.

Suppose that there is an information sequence $\vec{a} = (a_0, a_1, \dots, a_{K-1})$. Then coding this sequence to a sequence $\vec{v} = (v_0, v_1, \dots, v_{N-1})$ whose length is N . Sequence $\vec{v} = (v_0, v_1, \dots, v_{N-1})$ is used to transmitted in the channel and receiver could receive the information sequence $\vec{Y} = (y_0, y_1, \dots, y_{N-1})$ and then it will make a hard decision to get a new sequence $\vec{Z} = (z_0, z_1, \dots, z_{N-1})$ from $\vec{Y}$. The check matrix H of LDPC is $H = [\vec{h}_0, \vec{h}_1, \dots, \vec{h}_{M-1}]^T$, which $\vec{h}_i = (h_{i,0}, h_{i,1}, \dots, h_{i,N-1})^T$, $M = N - K$.

Using hard decision sequence Z and check matrix H to calculate syndrome vector $\vec{S}$, shown as bellow,

$$\begin{aligned} \vec{S} &= (s_0, s_1, \dots, s_{M-1}) \\ &= ZH^T \end{aligned} \quad (B.1)$$

$$= (z_0, z_1, \dots, z_{N-1}) \cdot \begin{pmatrix} h_{0,0} & h_{0,1} & \dots & h_{0,N-1} \\ h_{1,0} & h_{1,1} & \dots & h_{1,N-1} \\ \vdots & \vdots & \ddots & \vdots \\ h_{M-1,0} & h_{M-1,1} & \dots & h_{M-1,N-1} \end{pmatrix}$$

Which s_i is,

$$s_i = Z \cdot \vec{h}_i = \sum_{j=0}^{N-1} z_j h_{i,j}; \quad (B.2)$$

The addition functions above are Mod-2 add operation.

Vector S_i indicate whether the function is satisfied. If S_i equals to $\vec{0}$, then sequence Z is satisfied with the constraints relation of row i in check matrix. If vector $\vec{S}$ equals to $\vec{0}$ vector, means that all elements are satisfied with check matrix H then finally indicate that it got a exactly correct decoding sequence. Else there are non-zero elements in vector $\vec{S}$ indicates that there are some error bit in Z sequence and still should do more other processing. Using the vector S and check matrix H to calculate a new syndrome sequence F , then choosing the most unsatisfied function to reverse the relevant bit or bits.

$$\vec{F} = (f_0, f_1, \dots, f_{M-1})$$

$$= SH$$

$$= (s_0, s_1, \dots, s_{N-1}) \cdot \begin{pmatrix} h_{0,0} & h_{0,1} & \dots & h_{0,N-1} \\ h_{1,0} & h_{1,1} & \dots & h_{1,N-1} \\ \vdots & \vdots & \ddots & \vdots \\ h_{M-1,0} & h_{M-1,1} & \dots & h_{M-1,N-1} \end{pmatrix} \quad (B.3)$$

$$f_i = \sum_{j=0}^{M-1} s_j h_{j,i} \quad (B.4)$$

And here are the procedure of BF algorithm,

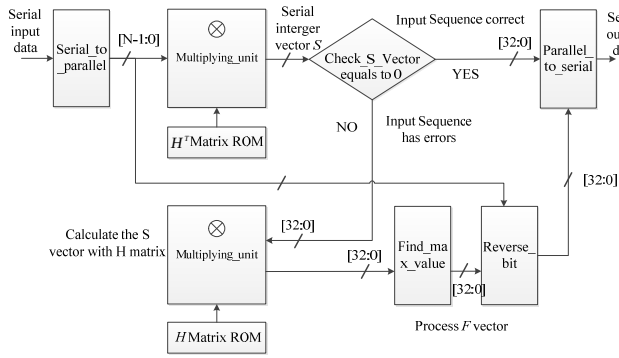


Figure 5. Block diagram of LDPC decoder algorithm

- (1) make a hard decision of input sequence ,if $y_n > 0$ then $Z_n^0 = 1$, else $Z_n^0 = 0$, so it will return out the initial decoding sequence $\vec{Z} = (z_1^0, \dots, z_N^0)$. The iterations is set to $k=1$;
- (2)multiplying Z^{k-1} with check matrix H^T , then result in the vector $\vec{S} = (s_1^{k-1}, s_2^{k-1}, \dots, s_m^{k-1})$;
- (3)counting the numbers of each node in $\vec{v}_n$ which is not equals to the check function $f_n^{k-1} = \sum_{m=1}^{K-1} S_m^{k-1}$;
- (4) If vector not zero vector $f_n^{k-1} = \sum_{m \in C(n)} S_m^{k-1}$ then multiplying $\vec{S}^{k-1}$ with check matrix H , then result in the vector $\vec{F}^{k-1} = (f_1^{k-1}, f_2^{k-1}, \dots, f_n^{k-1})$;
- (5)Finding the biggest element in vector $\vec{F}^{k-1} = (f_1^{k-1}, f_2^{k-1}, \dots, f_n^{k-1})$ and revert the information bit that the biggest elements corresponded then result is a new sequence;
- (6)Repeat the step 2 to step 5 until the elements in vector S are all satisfied with the check matrix H or the iterations gets the top value that system set.

III. RESULT AND ANALYSIS

By using Matlab to simulate LDPC of different length of 576, 1152 and 2304 at the condition of same code rate and 15 times of iteration. Then analyzing the influence of different length of LDPC to the BER performance. The result of simulation is shown as below,

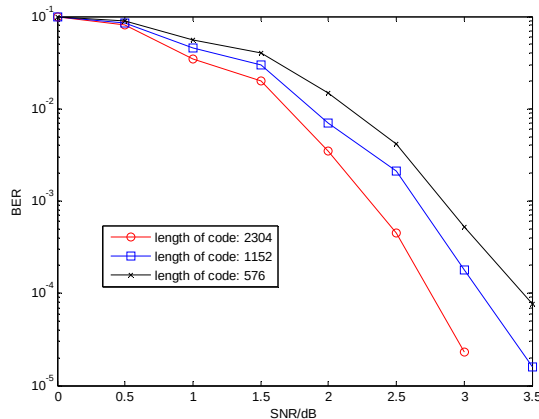


Figure 6. Comparison of BER in different length of 576, 1152 and 2304

From the Figure 6, it shows that the performance of LDPC is continuously improving with increasing of code length under the same SNB. In the low SNB area, it has little improvement to the BER when increase the length of code. But with the increasing of SNB, the BER of LDPC has been obviously reduced. At the BER of 10^{-4} , compared the code length of 1152 and 576 LDPC with 2304, the SNB has been decreased about 0.4dB and 0.8 dB. While with increasing of length, the improvement of performance is relative. When the length of code gets a relative value, the improvement of performance no longer increasing. For the reason that with the increasing of code length the complexity of coding and decoding also increased, and the LDPC performance will approach the limitation.

By using Matlab to analysis the 576 length, code rate of 3/4A LDPC with the different iteration of 5, 15 and 30. The result of simulation from Matlab in different iteration of LDPC shown as below,

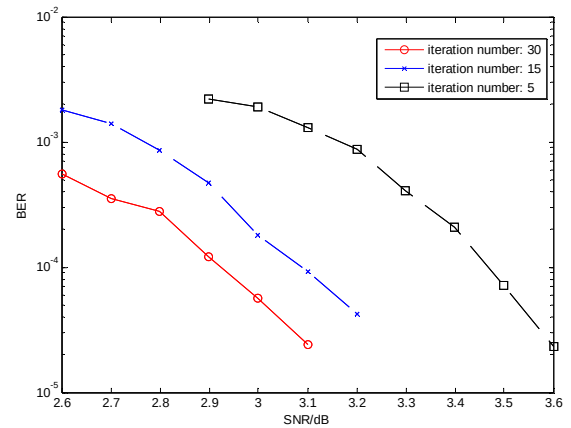


Figure 7. BER & SNB in different iterations of 5, 15 and 30

From the Figure 7 it indicates that under the same SNB the performance of LDPC improved with the increasing of iteration times. At the BER of 10^{-4} , compared the iteration of 15 and 5 times with 30 times, the SNB has been decreased about 0.2dB and 0.5 dB respectively. But the BER of LDPC couldn't keep decreasing unlimitedly with the increasing of iteration times. No matter how to increase the iteration the performance of LDPC wouldn't improve, when the BER has decreased to a limited level. At this time the increasing of iteration only make the coding or decoding much more complicated.

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