An Experiment Design for Measuring Response Time of FPGA Logic Cell

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***Abstract*—Response time of digital device affects signal competitions and hazards seriously, and these competitions and hazards often cause instability and error of instruments, so response time of FPGA logic cell is a very important parameter of the chip, especially in high speed FPGA signal processing system. Because response time of most logic devices is very short, its measurement is always difficult. In this paper, an ingenious method of measuring response time of FPGA logic cell is put forward. A measurement experiment is designed, and its measuring principle is analyzed. The experiment testified the correctness of the method of response time measuring.**

Keywords—FPGA, Response time, Measurement

I. INTRODUCTION

Signals can be processed at a high speed because every unit in FPGA (Field Programmable Gate Array) chip can operate in parallel. So FPGA had been widely used in many kinds of instruments‟ design in recent decades. The more quickly a signal is processed, the more competitions will happen, and the more hazards may arise. At the same time, the longer response time the device has, the more hazards may arise too. Competitions and hazards always cause instrument instability or error. Considering competitions and hazards in very important in instrument design, especially in high speed digital circuit system. In the course of researching high speed digital multichannel analyzer in our science research project, the design experiment failed many times because of the competitions and hazards. So more efforts must be made to avoid them. Response time of most logic devices is often very short, its scale is always from fractions of a nanosecond to nanoseconds depending on technology, fan-in, fan-out, and so on. The response time can not be the exactly same for any two devices, even of the same type [1]. The device‟s response time is one of key factors for instrument operation speed and reliability. Because the response time is very short, measuring response time is not an easy thing. How quickly can FPGA chips operate on earth? In this paper, taking a counter as an example, a method of measuring response time of FPGA logic cell is put forward. A measurement experiment is designed and its principle is analyzed as follows.

II. MEASUREMENT OF RESPONSE TIME OF FPGA LOGIC CELL

Most logic function circuit can be implemented using Configurable Logic Blocks(CLBs) by means of programming in FPGA. CLBs are fundamental programmable functional element of Spartan family architecture. CLBs contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data [2]. A counter is taken as an example of a FPGA logic cell to measure the response time.

A. Principle of the measurement

The following three methods can measure the response time of a counter in FPGA. The first method is measuring the counter‟s counting times in a given time. The second one is measuring the operating time when the counter‟s counting times is given. The third one is measuring the response time via oscilloscope directly.

1) Measure counting times in a given time

A gate control time with given width is set as *T*. During this gate control time, the counter operates continuously; on the contrary, in the rest of the time, the counter doses not count. The measurement principle is shown as Fig.1.

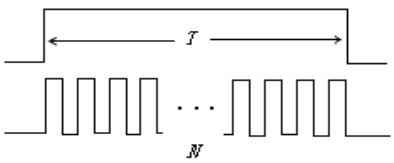

Fig. 1. Principle of measuring counter‟s response time

If the operation times *N* of the counter in the given time is measured, the average response time *t* of the counter can be calculated via the operation times *N* and the width of gate control time *T*. The average response time *t* is expressed as the following equation

$$t = \frac{T}{N} \tag{1}$$

2) Measure operating time with given counting times

A counter is designed. We make the counter count given times *N* continuously, so the counting times is known. At the same time, the counter‟s operating time *T* can be measured when the counter counts *N* times. The average response time *t* can be calculated through formula (1) too.

3) Measure with oscilloscope directly

This method is to measure the response time with oscilloscope directly. A counter is designed, and this counter can operate continuously. We can measure the frequency or period of any one bit of the counter. The response time can be calculated through the frequency or period.

B. Experiment design

In this experiment, a Digilent BASYS-2 Xilinx FPGA developing board is used. The core chip in this board is XC3S100E. The clock pulse frequency is 50MHz.

1) Experiment design based on measuring counting times

Firstly, we set a gate control signal with given width. This gate control signal “gate” can be described in VHDL [3] as follows.

```
-------------  gate set  -----------------
  process(clk)
     begin
        if(falling_edge(clk)) then
           if clkdiv <= m then
              clkdiv <= clkdiv + 1;
              gate <= '1';
           else
              if clkdiv <= 50000000 then
                 clkdiv <= clkdiv + 1;
                 gate <= '0';
              else
                 clkdiv <= x"00000000";
              end if;
           end if;
        end if;
  end process;
-----------------------------------------
```

The frequency of clock pulse “clk” of this developing board is 50MHz, so the clk‟s period is 20ns. In this program, when “clkdiv” is less m, there are m pulses altogether, so the gate control width *T* is m*20ns. In the course of this time, the gate control signal “gate” is „1‟, and in the rest of time, “gate” is „0‟. So the width of this gate control time *T* is set as *m**20ns. And the gate control signal can be generated once per second.

Secondly, a counter is designed, which counts continuously in the gate control time and does not count in the rest of time. The counter can be described as follows.

```
-----------   COUNT N   -----------------
  process(gate)
     begin
       if(gate = '1') then
          N_CNT <= N_CNT + 1;
          N <= N_CNT;
       else
          N_CNT<= x"0000";
       end if;
  end process;
-----------------------------------------
```

As shown in the above program, when the gate control signal is „1‟, the counter is enabled, at this moment the counter N_CNT will count continuously. On the contrary, when the gate control signal is „0‟, the counter will not count. After the gate control, the result of the counter *N* is outputted. The value of *N* is just the counter‟s operation times in the given time *T*. So counter‟s response time *t* can be calculated via *T*/*N*. Because clock pulse is generated via crystal oscillator, the pulse frequency is very stable, so the time width error of *T* can be ignored when it is compared with the logic cell‟s response time error. That is to say, *T* can be regarded as an accurate value in response time calculation.

In the above experiment, if m is set as 100, there are 100 pulses in the gate control, so the width of gate is 2000ns. In this condition, the counter counting times is shown in Fig.2.

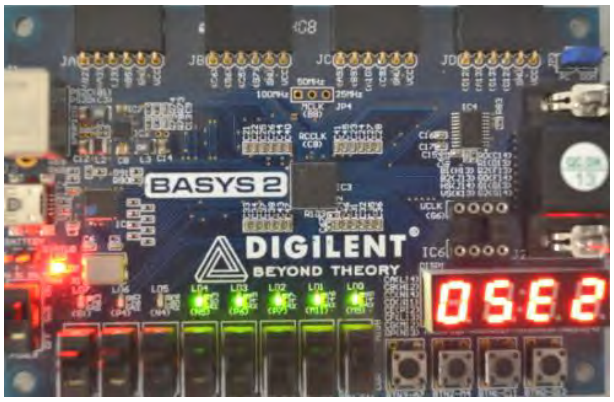

Fig. 2. Count number in 2000ns

According to Fig.2, the number that leds display is “05E2”. This number is a hexadecimal value of *N*. This hexadecimal number can be transformed to a decimal number “1506”. Then we can know that the counter counts 1506 times in 2000ns. So the response time can be calculated as 1.328ns.

When *m* is set as other values, the result of the experiment is shown in Table.I. Because the numbers of counting times fluctuate in a small range, in this table, each number of *N* is an average value of five random readings.

TABLE I. EXPERIMENT RESULT OF MEASURING COUNTING TIMES

Experiment No.	*m*	gate width *T*/ns	counting times *N*	*t* /ns
1	100	2000	1506	1. 328
2	200	4000	3003	1. 332
3	300	6000	4507	1. 331
4	400	8000	6021	1. 329
5	500	10000	7532	1. 328
6	600	12000	9020	1. 330
7	700	14000	10519	1. 331
8	800	16000	12031	1. 330
9	1000	20000	15028	1. 331
10	2000	40000	30022	1. 332

From the result of the above table, we can see the FPGA counter"s response time *t* is about 1.33ns in current condition. That is to say, counting once needs 1.33ns. The response time is not entire same in every experiment, but the change is very small. The magnitude of result is just the scale of FPGA logic cell"s response time, and the result is stable by and large, so the result is credible.

2) Experiment design based on measuring operating time

A counter is design as follows. The counter N_CNT will count *N* times continuously. The counting interval is just a response time of the counter.

```
---------  N times counting   -----
process(timer_1s)
   begin
     if timer_1s = '1' then
       if N_CNT <= N then
         N_CNT <= N_CNT + 1;
         gate <= '1';
       else
         gate <= '0';
       end if;
     else
       N_CNT <= x"00000000";
       gate <= '0';
     end if;
 end process;
-------------------------------------
```

In the course of *N* times counting, the gate is evaluated "1"; on the contrary, it is evaluated „0". So the width of gate is the same as the width of the counter"s counting time.

Another counter is designed as follows to measure the width of the gate.

```
---------  COUNT TIME  -------------
 process(clk)
    begin
      if(falling_edge(clk)) then
        If gate = '1' then
           M_CNT <= M_CNT; + 1;
           M <= M_CNT;
        else
           M_CNT; <= x"0000";
        end if;
      end if;
 end process;
-------------------------------------
```

From the above process, there are *m* pulses in the course of gate, so counting time is *m**20ns. The result of the experiment is shown in Table.II. In this table, every value of *m* is the average value of five random readings too.

TABLE II. EXPERIMENT RESULT OF MEASURING OPERATING TIME

Experiment No.	counting times *N*	*m*	counting time *T*/ns	*t* /ns
1	5000	327	6540	1.308
2	10000	654	13080	1.308
3	20000	1309	26180	1.309
4	30000	1962	39240	1.308
5	40000	2618	52360	1.309
6	50000	3274	65480	1.310
7	80000	5235	104700	1.309
8	100000	6545	130900	1.309
9	200000	13079	261580	1.308
10	500000	32730	654600	1.309

According to Table.II, the average response time of the counter is about 1.31ns. This value is approximately equal to the one of the former result.

3) Experiment design of measuring with oscilloscope directly

A counter is designed too. This counter will count continuously all the time. If any bit of the counter is outputted, we can measure the frequency or period of the output signal with oscilloscope directly. For example, when we measure the frequency and period of counter(10), we can get the average frequency is 432.5 kHz, and the average period is 2.312 μ s. The frequency of counter(0) is 1024 times the one of counter(10), and the period of counter(0) is one 1024th the one of counter(10). Moreover, a period contains of two times state conversions. So we can infer that the response time is 1.129ns. This value is somewhat different from the former ones. The difference is mainly from different fan-out.

From the above three methods, the response time values are approximate equal. And the value of the response time is stable on the whole in every method of experiment. There are some differences among the above methods. These differences mainly come from different circuits that are generated from different program, such as fan-in, fan-out and logic cell.

According to similar principle, if an experiment is made by means of not gate circuit ring vibrator, the response time of not gate circuit can be measured too.

III. CONCLUSION

As can be known from the above analyses, through adopting three measuring methods and setting different parameters, FPGA counter"s response time is measured accurately. The result shows this means of experiment is feasible. If some similar methods are used, the response time of other FPGA logic cells can be measured accurately too. The experiment testified the correctness of the method of measurement.

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