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An Ultra Low-power Low-Voltage Programmable Frequency Divider for PLL Frequency Synthesizer

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***Abstract*—In this paper, an ultra low-voltage frequency divider for PLL (Phase Locked Loop) was designed using 0.13um CMOS process with 0.6V power supply. The frequency divider employs divide by 15/16 dual modulus prescaler based on phase switching, two programmable counters and the control module for prescaler. The operation frequency of this divider is from 0.8GHz to 2.2GHz. The power dissipation of the programmable frequency divider is only equal to 603uW. Additionally, a PMOS VCO oscillator from 1.51~1.70GHz was designed to cooperate with the programmable frequency divider which consumes 660uW from 0.6V supply voltage.**

Keywords—Frequency divider; Low-power; Low-voltage; Phase switching; 0.13um COMS

I. INTRODUCTION

A growing number of wireless communications equipment such as GPS, WIFI and Blue Tooth are essential for People's Daily life. Frequency synthesizer is a crucial unit for wireless communication systems [1]. PLL frequency synthesizer has the advantage of simple structure, mature, high purity of the output spectrum. Therefore, PLL synthesizer is the most widely used way to generate the local oscillating signal. Fig.1 shows a conventional integer charge-pump PLL with a programmable divider.

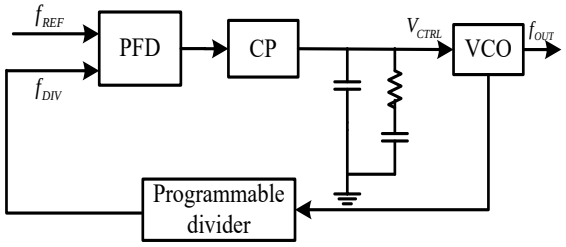

Fig.1 The block diagram of the charge pump PLL

Low-power technology is very important for wireless communication system for battery supply. The frequency synthesizer based on PLL in radio frequency (RF) transceiver consumes excessive power [2], hence, its low-power design is essential. Programmable divider and voltage controlled oscillator (VCO) occupied vast majority power of PLL for their high operating frequency[3,4]. Low supply voltage is one important approach to reduce the power consumption. The ring oscillator and the LC oscillator are the two common scheme for integrated circuit design. The ring oscillator has smaller area and power dissipation but poor performance in phase noise. The LC oscillator has been widely used in wireless communication systems for its good performance in phase noise. Especially, the PMOS VCO has lower transconductance but better performance in flicker and white noise [5-7].

In this paper, a low-power low-voltage programmable divider with 0.6V supply and 603uW power dissipation is presented. Besides, a 0.6V supply PMOS VCO consumes 660uW was designed to cooperate with the divider.

II. CIRCUIT DESIGN

A. Programmable frequency divider

Programmable frequency divider plays an important role in PLL frequency synthesizer. It operates at a high frequency and consumes lots of power dissipation. The conventional architecture of programmable frequency divider is pulse swallow architecture or cascaded by 2/3 cells. Owing to the frequency division ratio of pulse swallow frequency divider can be modified through the preset number, the adjusting range is very large than other architectures and it can meet the need of the high frequency. Therefore, the pulse swallow frequency divider is widely used in PLL.

The block diagram of the programmable frequency divider architecture in this paper is shown in Fig. 2. The programmable frequency divider takes pulse swallow architecture. It is composed of a 15/16 dual modulus prescaler and two programmable counters. The prescaler consists of one dynamic logic (DL)[8] divide-by-2 stage, one source coupled logic (SCL) divide-by-2 stage, one true single phase clock (TSPC) divide-by-4 stage and one module for phase switching. The prescaler is controlled by the programmable counter for continue frequency dividing ratio. As shown in Fig.2 when the SEL is low the AND will be locked up and the prescaler will operate at divide-by-16 stage, otherwise operate at divide-by-16 stage. The P and S counter is two programmable counters which determine the programmable divide ratio and provide the control signal for prescaler. The divide ratio range for this programmable divider is 60~240.

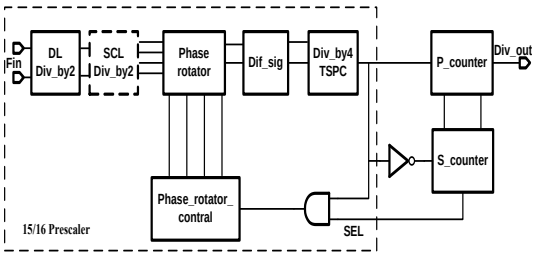

Fig.2 The block diagram of the programmable frequency divider.

The most power dissipation is on the prescaler for its high operating frequency. Therefore, the divider after Phase rotator adopts TSPC structure which input frequency range from 200MHz to 550MHz. And under the 0.6V supply voltage the operating frequency is also limited by the first level divide-by-2 stage. To get the low power, low voltage and high operating frequency the first divide-by-2 stage was implemented by DL divider propose in [8].

The schematic for the DL frequency divider with single-clock D flip-flops is depicted in Fig.3.In this divider, two identical D flip-flops controlled by a single input signal (CLK/CLKB) coupled with each other. The dc bias of clock signal should be biased closed to 0V to get a minimum supply voltage. The max operation frequency of this architecture is much higher than the conventional SCL structure. Therefore, the first divider is chosen this architecture for low voltage and high frequency design. However the dc bias of the output in DL divider is closed about 300mV which makes the cascading of these dividers impossible at low supply voltage. Hence, the second divide-by-2 stage we chose the SCL divider for the half operation frequency.

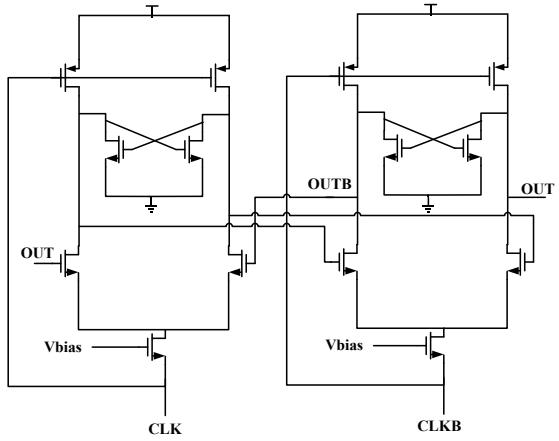

Fig.3 The schematic for the DL frequency divider

B. *VCO Design*

A high performance voltage-controlled oscillator (VCO) is another key component of PLL frequency synthesizer front-end circuits. The design of VCO is extremely critical, since it requires a tight trade-off between high tuning linearity, low power, low phase noise, low flicker noise and wide tuning range[9-11].

For this design the closed to 0V dc bias was desired for the first level divider input signal. A PMOS cross-coupled VCO was designed in this topology to cooperate with the programmable divider. The schematic of VCO is shown in Fig. 4.

In this topology, an appropriate Vbias should be a cautious choice to make trade-off between power consumption and the transconductance of the MOSFET. The dc bias of VCO outputs is around 0V and the amplitude can be almost 1V for single-end output. The nmoscap varactor is used to get a large tune range. The tune voltage of this VCO is 0~0.6V and the frequency tuning range can be 1.51~1.70GHz.

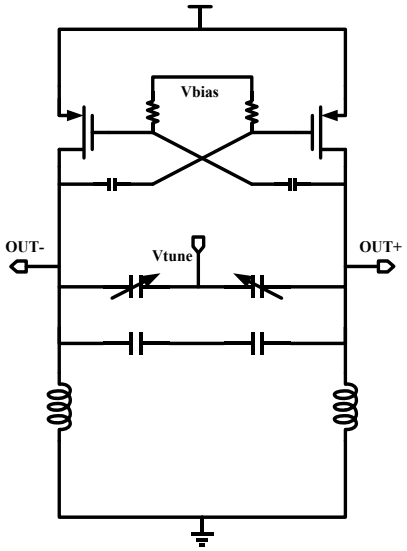

Fig. 4. Schematic of PMOS VCO

III. Simulation Results

The proposed programmable frequency divider and VCO block are simulated in TSMC 130nm process with 0.6V supply voltage. Primarily, we simulated Programmable frequency divider and VCO respectively. From the simulation results we found that the range input frequency of our frequency divider can operate at 0.8GHz~2.2GHz when the dc bias is 0V no whether the process corner is 'ss', 'tt' or 'ff' and the swing is about 0.3V single-end at 'tt' corner. The power consumption in 'tt' corner of programmable frequency divider and VCO is 603uW and 660uW respectively. Eventually, we also simulated by combined them together. When we simulate the VCO with driving the frequency divider, the oscillate frequency and the output the amplitude of the VCO output will be little small because of the parasitic capacitance. The simulation results show that our design have little lower power and little lower output amplitude in 'ss' corner than it in 'tt' corner. And the simulation in 'ff' corner have the opposite result. There are some details of our simulation in 'tt' corner which combine frequency divider and VCO together will be demonstrated in this section.

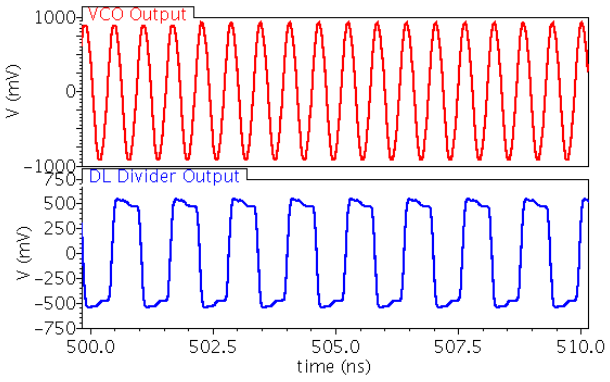

Fig.5 The waveform of VCO and DL divider

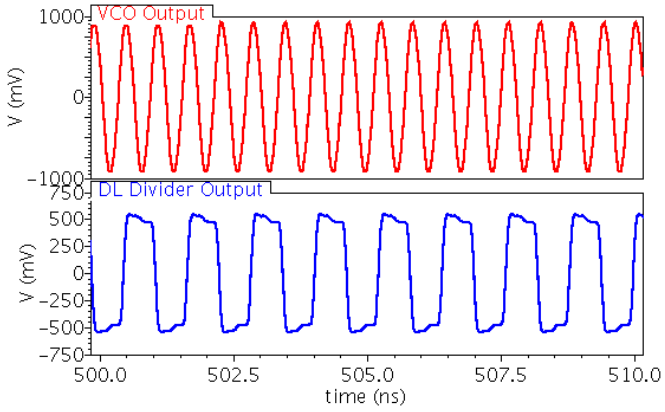

Fig.6 The waveform of Phase-rotator output and the Prescaler output

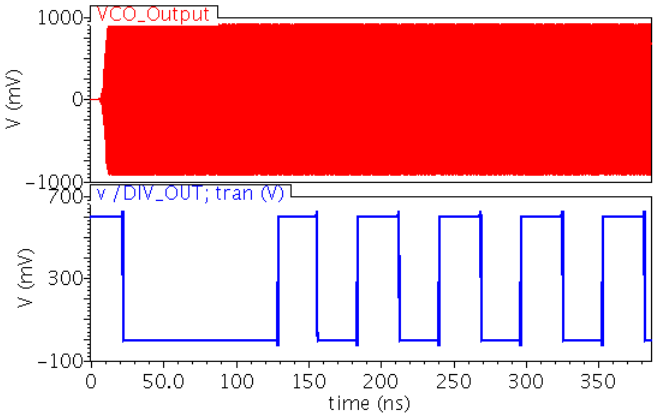

Fig.7 The waveform of VCO and the programmable divider

In the simulation the VCO oscillate on 1.685GHz and the divide ratio of programmable frequency divider is 95. The differential waveform of VCO and DL divider are shown in Fig.5. From the results we can found that the amplitude of DL divider output can reached above 500mV in 0.6V supply. This is beneficial for subsequent operation in the circuit. And the waveform of the output of other modules in the programmable frequency divider and the output of all the programmable frequency divider is depicted in Fig.6 and Fig.7.

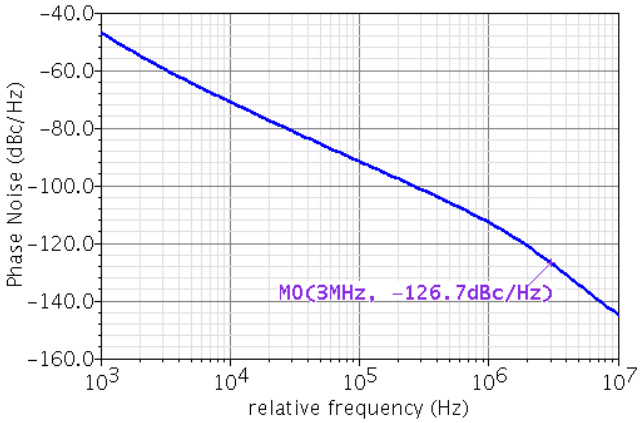

Fig .8 The phase noise simulation results of VCO

A 'pss' simulation result of VCO is shown in Fig.8 and Fig.8. The phase noise of the PMOS VCO is -126.7dBc/Hz @3MHz as depicted in Fig.8. The tuning range of this VCO is 1.51~1.70GHz with the tuning voltage from 0V to 0.6V. And the VCO has an impressive tuning linearity which is shown in Fig.9.

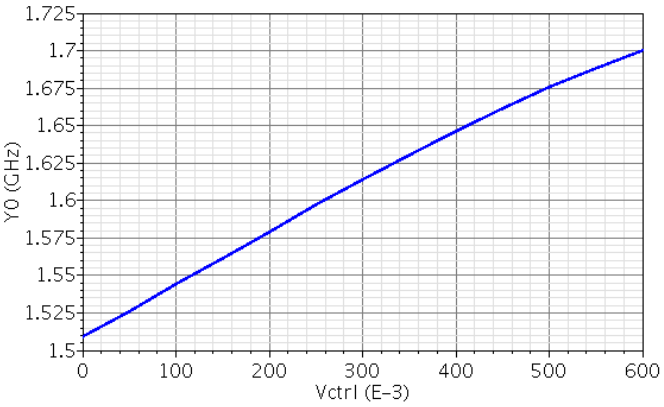

Fig .9 The tuning curve of VCO

IV. Conclusion

In this paper, an ultra low-voltage and ultra low-power programmable frequency divider and VCO is designed for PLL frequency synthesizer. The programmable frequency divider can operate from 0.8GHz to 2.2GHz which consumes 603uW with 0.6V supply voltage. The PMOS VCO was designed to cooperate with the frequency divider which tuning range is 1.51GHz~1.7GHz. The phase noise of the VCO is -126.8dBc/Hz @3MHz and the power dissipation is 660uW.

Acknowledgment

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