A Design of Frequency Synthesizer based on DDS for Ka-band Radar Signal Simulation

Weiliang Gao*, Dalong Li and Dong Xia
The Qingdao Branch Campus of Naval Aeronautical University, Qingdao 266001, P.R.China
*Corresponding author

***Abstract*—This paper puts forward a design of frequency synthesizer based on DDS for Ka-band radar signal simulation. RF signal is generated through the AD9854 DDS chip driving the PLL and VCO. The testing results showed that this Ka-band frequency synthesizer has low phase noise and wider bandwidth, and can generate Ka-band continuous wave signal, LFM signal for radar signal simulation.**

Keywords—DDS; Ka-band; frequency synthesizer

I. INTRODUCTION

The frequency source is the core of modern radar system, in order to meet the need of all-phase reference, the radar signal generator must have the higher performance in wider band. In recent years, the development of DDS (Direct Digital Synthesizer) and PLL (Phase-Locked Loop) technique, provides a better method to design the higher performance frequency synthesizers. This paper puts forward a design of frequency synthesizer based on DDS for Ka-band radar signal simulation. The output of VCO (Voltage Controlled Oscillator) , which is a part of PLL , is phase locked by DDS. By driving PLL through the DDS, we can obtain the higher performance Ka-band continuous wave signal and LFM signal.

In the Paragraph II, this paper provides the Structure of DDS driving PLL frequency synthesizer and designs the schematic circuit diagram. In the Paragraph III, the phase noise and frequency capture time are analyzed by simulation. The test and measurements results are given in Paragraph IV.

II. ENGINEERING IMPLEMENTATION

A. The Structure of Frequency Synthesizer

The Structure diagram of DDS-driving PLL for Ka-band frequency synthesizer is shown in Figure I. The crystal oscillator produces the reference frequency of DDS, f_{ref} , f_{DDS} is the output frequency of DDS and is controlled by the frequency tuning word *K*. The reference frequency of PLL is driven by the f_{DDS} . The Charge Pump (CP) controls the output of VCO. We can get the output signal of this frequency synthesizer by multiplying $f_{VCO} \cdot f_{diejia}$ is the LFM signal and the additional Doppler frequency signal.

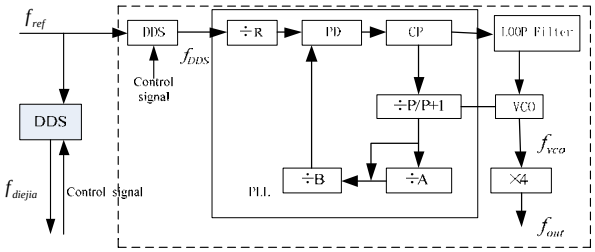

FIGURE I. THE STRUCTURE DIAGRAM OF DDS-DRIVING PLL FOR KA-BAND FREQUENCY SYNTHESIZER

While The PLL is locked, the output frequency of frequency synthesizer and the VCO is

$$f_{out} = 4 \times f_{vco} \tag{1}$$

$$f_{VCO} = (BP + A) \times \frac{f_{DDS}}{R} \tag{2}$$

f_{DDS} vaties with the frequency tuning word *K*, and

$$f_{DDS} = \frac{K}{2^N} \cdot f_{clock} \tag{3}$$

Where *N* is the phase accumulator word length of DDS and f_{clock} is the internal clock of DDS. We can substitute the equation (3) into (2), then f_{VCO} can be expressed as

$$f_{VCO} = \frac{A + BP}{B} \cdot \frac{K}{2^N} \cdot f_{clock} \tag{4}$$

In the Structure shown in Figure II, due to the good frequency resolution ratio of DDS chip, the frequency resolution ratio of the output signal can be found from (4) to be superior to traditional Structure.

With DDS, LFM signal and Doppler frequency signal can be generated easily. In the LFM mode, the output of DDS, f_{com} , can be expressed as

$$f_{com} = \frac{K + \Delta K \times t}{2^N} \times f_{clock} \tag{5}$$

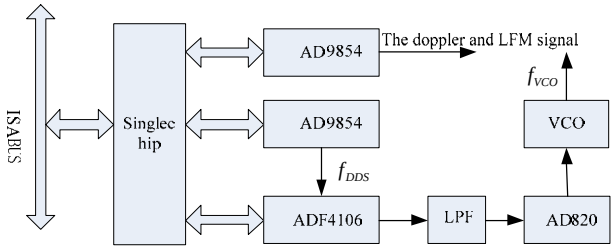

FIGURE II. THE CONTROL CIRCUIT SINGLE CHIP

Where ΔK is the change rate of frequency tuning word K . t is the time of duration of pulse of LFM signal. From the equation (5), the Doppler frequency f_d is

$$f_d = \frac{K}{2^N} \times f_{clock} \tag{6}$$

The band B of LFM signal is

$$B = \frac{\Delta K \times t}{2^N} \times f_{clock} \tag{7}$$

B. *The Circuit Design*

This design implements the low phase noise level signal generating, the center frequency is required 35GHz, the band is 3 GHz, the frequency resolution ratio is 100kHz, the phase noise level is less than -85dBc/Hz @1kHz. From the equation (1) , the f_{VCO} is required 8.375GHz~9.125GHz, The band B of LFM signal is 150MHz. According to the design requirement, we use the AD9854 DDS module and ADF4106 PLL device to design the circuit. The Single chip can receive the data which come from the ISA bus and write the FTW to the AD9854, which make AD9854 produce the frequency signal.

We use the Single Chip of µPSD3251 to provide the write time diagram, which is shown in Figure III.

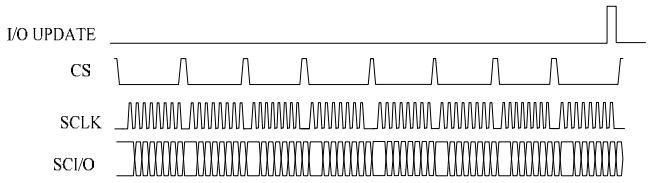

FIGURE III. THE WRITE TIME DIAGRAM OF SINGLE CHIP

By doubling the external reference clock, we make the internal clock of AD9854 reach 300MHz. It can easily generate low frequency LFM signals with better dynamic performance. The ADF4106 has a wide band, which consists of a programmable reference divider, a digital phase frequency detector (PFD), programmable dual-modulus prescaler, a precision charge pump. It has fast settling time and low phase noise performance. The loop filter design can remove the high frequency component and ensure the loop stability. The AD820 amplifier is used to design the loop filter.

III. ANALYSIS AND SIMULATION

By using the ADI SimPLL software, which can calculate the phase noise curve and the capture time, the performance of the designed frequency synthesizer is analyzed and evaluated.

A. *Phase Noise*

The output phase noise is simulated at the central frequency 35GHz. The result of simulation is shown in Figure IV. We find that the phase noise level at -87dBc/Hz@1kHz and at -140dBc/Hz@1MHz, which verifies the frequency synthesizer has a good phase noise performance and meet the designing need.

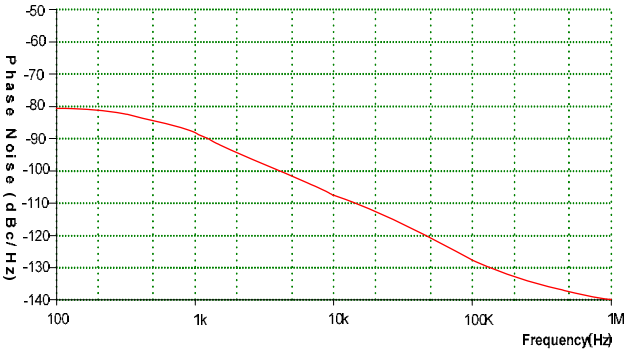

FIGURE IV. THE PHASE NOISE CURVE

B. *Capture Time*

The capture time is the time of the frequency synthesizer change the frequency from one frequency point to another frequency point. The capture time is decided by the PLL, which will be faster locked when the PD works on the higher frequency. We make the simulation when the locked frequency is 35GHz. The result is shown in the Figure V.

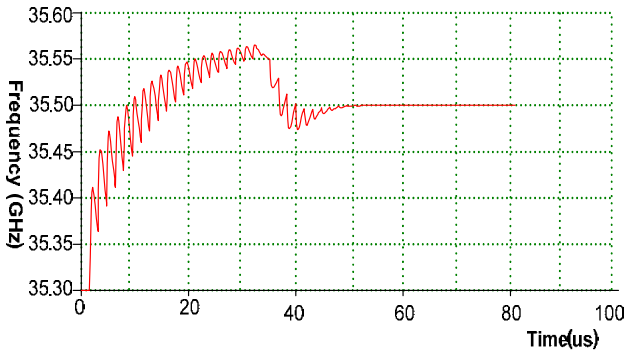

FIGURE V. THE CAPTURE TIME

IV. EXPERIMENTS AND MEASUREMENTS

In order to test the performance of the Ka-band frequency synthesizer given in this paper, we use the frequency synthesizer to produce the single frequency continuous wave signal, the modulated frequency signal and LFM pulse signal.

A. *The CW Signal*

A CW (Continuous Wave) signal of VCO at 8.75GHz is produced using the frequency synthesizer. The spectrum is shown in the Figure VI.

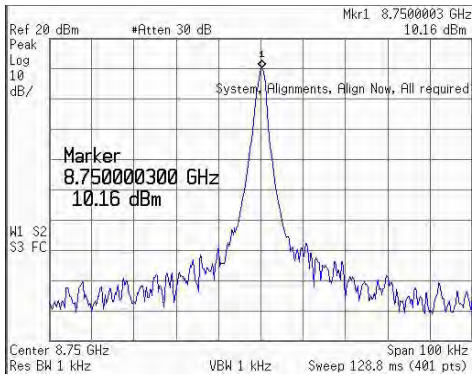

FIGURE VI. THE CONTINUOUS WAVE SIGNAL AT 8.75GHZ

The output signal is the four frequency multiplication of the f_{VCO}, the f_{out} is shown in the Figure VII. The f_{out} can be changed from 33.5GHz to 36.5GHz, the phase noise level is less than -85dBc/Hz@1kHz.

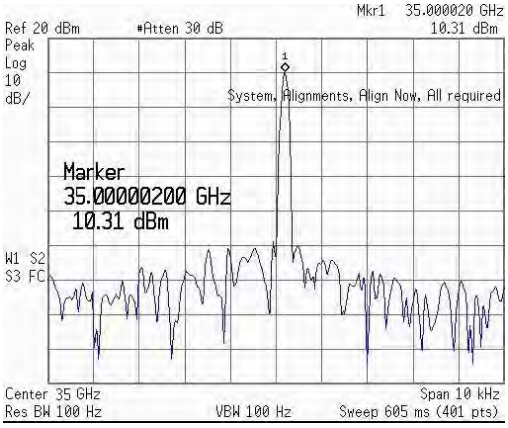

FIGURE VII. THE FREQUENCY SPECTRUM OF 35GHZ CONTINUOUS WAVE SIGNAL

B. The Modulated Frequency Signal

A pulse modulated frequency signal is produced and measured. The frequency spectrum is shown in Figure VIII.

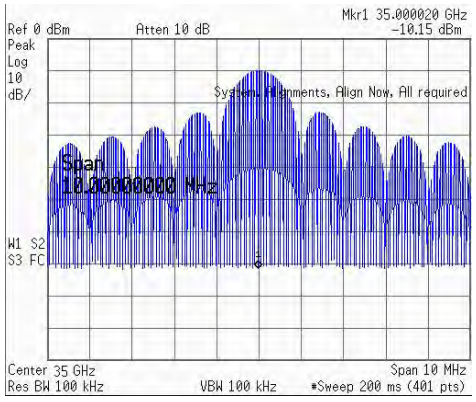

FIGURE VIII. THE FREQUENCY SPECTRUM OF 35GHZ MODULATED SIGNAL

C. LFM Pulse Signal

A linear FM pulse signal is produced and measured. The frequency spectrum is shown in Figure IX. The linear FM pulse width is from 10μs to 50μs, The linear FM bandwidth is from 10 MHz to 150 MHz.

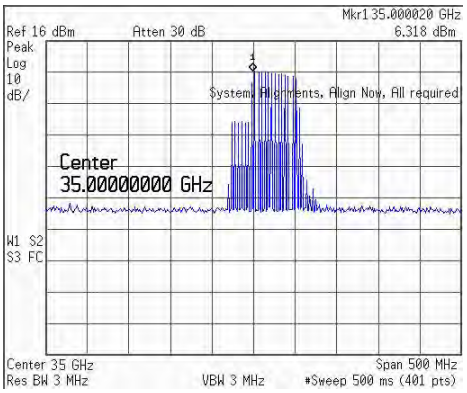

FIGURE IX. THE FREQUENCY SPECTRUM OF LINEAR FM PULSE SIGNAL

V. CONCLUSION

This paper provides using the AD9854 DDS module and ADF4106 PLL device to design a Ka-band frequency synthesizer. The circuit diagram is given and its performance is analyzed. Experiments results shown that the Ka-band frequency synthesizer has wider bandwidth and better performance and can be used to produce multiple radar signals for simulation, such as CW signal, the modulated frequency signal and LFM pulse signal. It meets the demand of Ka-band radar signal simulation.

REFERENCES

[1] AD9854 Datasheet. Analog Device Inc, 2000.Cicero S.

[2] ADF4106 Datasheet, Analog Device Inc, 2005.

[3] Dean Banerjee., PLL Performance, design and simulation. National Semiconductor. 1998

[4] Vaucher, “An Adaptive PLL Tuning System Architecture Combining High Spectral Purity and Fast Settling Time”, IEEE journal of solid-state circuits, Vol. 35, NO. 4, APRIL 2000.

[5] Fei Yuanchun, Su Guangchuan, Mi Hong, etc. “The generating technology of wideband radar signals”. National Defense industry press. 2002.1(In Chinese)