In the design, the Ping-Pong operation is to achieve seamless buffering, improve the data output rate. This module consists of two MUX and two DPRAM, through to the multiplexing of function module, in order to achieve the target which is improving the operating rate.

4. Simulation and Verification of CAVLC Encoder

Using the sequence of standard test: 0, 0, 5, 3, 2, -1, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, and the NC value is 3, using the design of the CAVLC encoder to simulation by Modelsim SE 6.5, and the results as shown in Figure 4. In the figure, when trans_go is 1, it's said the output value is effective when the next clock cycle is come; when trans_over is 1, it's said the output value is end when the next clock cycle is come. The bitstreams of data_out port is the output of CAVLC encoded.

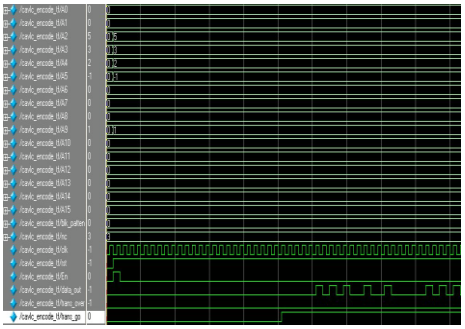

Figure 4: The simulation results

The output is the encoding through manual look-up table: 00001011000100101010101111, the results and the results of CAVLC encoder is same, thus verify the correctness of the CAVLC encoder.

5. Conclusion

This paper gives the analysis of CAVLC encoding algorithm in the H.264/AVC standard, and to solve this problem that the algorithm complexity is high and not easy to achieve require of real-time, and the paper put forward a high speed system for CAVLC encoding of H.264 standard. In this system, programming with Verilog HDL achieves the hardware circuit, and through FPGA to validate the correctness of the design. The highest of frequency is up to 148.67MHZ in this system, it can satisfy the requirement of real-time about HD video, and the design has a greater of significance in engineering practice.

6. References

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