Design of Three-phase Multifunctional Power Quality Online Monitor Based on SOPC

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Abstract

A multifunctional Power Quality Online Monitoring System was designed. The System takes FPGA as core, assisted by signal Acquisition and Processing, data storage, display and communication interface circuit. It also utilizes the FAFT algorithm to calculate harmonic waves of three-phase network. The design scheme of software and hardware was give, he the experiment shows that the monitor can measure the effective value and harmonic components of three-phase voltage and current, three-phase unbalance, active power, reactive power, power factor, supply frequency and so on.

Key words: power quality; on-line monitoring; FAFT

1. Introduction

Electric energy is the most important energy in our society, it is the stability and security of the power grid and the level of power quality that have been the important influencing factors to the development of the national economy[1-2]. Comprehensive management of the grid must carry out a omni-directional testing on user network to obtain the essential parameter of grid. With the development of programmable logic device, the technology of System on a Programmable Chip (SOPC) has been widely applied in the fields of electronics, communication and industry control and so on[3]. This paper provides a design program of the power quality analysis system based on SOPC technology, which makes it have the best portability and the highest cost performance ratio, and promote the real-time monitoring of the grid parameters and the development of the power quality management work when applying the latest technology.

2. Structure Design

The power quality monitor can be generally summarized into four parts: hardware platform of the grid parameters monitoring system based on FPGA, Acquisition and Processing circuit for grid signal, high speed A/D circuit and keyboard and liquid crystal display circuit. As shown in Fig.1.Put soft Core CPU NiosII as the control core, FAFT IP Core as the core of the grid harmonic analysis within the FPGA. Meanwhile, some other user defined IPCore should also be included, such as UART used to communicate with PC, A/D conversion module, figure wave filtering module FIR, which make the system highly integrated. the main working process of the whole system is shown as follows:

It is the CT/PT sensor units that gain the three-phase voltage and current signals, when the system completes its initialization of each unit after starting.

Through the phase-locked frequency multiplier synchronous circuit tracking the real-time operating frequency of power line, the units use one of the voltage signals to control the sampled signals converted with A/D, which makes the A/D circuit carry out 6-channel signals conversion synchronously within a period of operating frequency, and brings the conversion results into the FIR filter to be filtered, then the filtered digital is stored in the cache of double-port RAM. While FFT, started by the NiosII controller, reads data from the double-port RAM, finishes 128 points 6-channel signals' FAFT data processing, gets amplitudes of each harmonic wave. NiosII, at the same time, reads data from the double-port RAM and performs power parameters calculation. Finally, the NiosII controlling system reads the analysis results, and then displays the results on the LCD, or transmits them out through the communication interface.

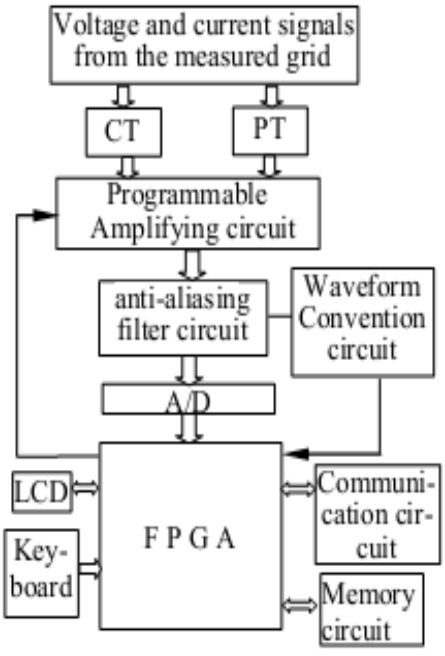

Fig. 1: system hardware composition

3. Hardware Design

3.1. A/D conversion circuit

In order to ensure the grid's safe operation and real-time detection, analyze all of its operation parameters, the system chooses the chip ADS7864, which is the fastest 6-channel fully- input double 12-bit A/D converter[4]. data acquisition module is the IP core which is written by the VHDL. Take the output signals from the phase-locked frequency multiplier circuit as the sampling trigger pulses CLK of the ADC controller, and the digital frequency multiplier signals, every time, output an effective sampling trigger signal CLK, the ADC controller will complete a 6-channel sampling operation, then stopped to wait for arriving of the next trigger pulse. The data sampling module structure diagram is shown in Figure 2.

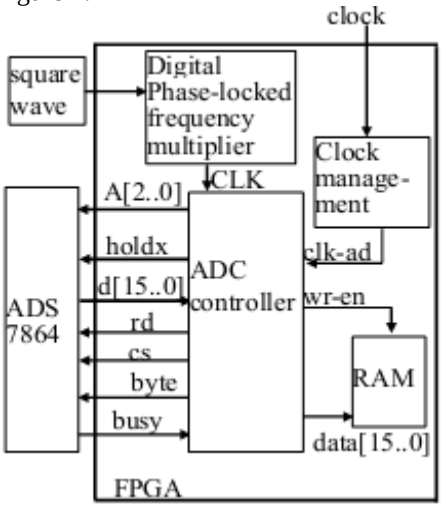

Fig. 2: data acquisition interface diagram

3.2. Harmonic Analysis

The traditional harmonic analysismethods generally make the discretization of measured signals to be processed with the classical Fast Fourier Transform(FFT), to get each harmonic signal amplitude, frequency and phase, but because the

sampling period is not synchronized with the signal cycle and the sampling frequency is limited, strict synchronization is difficult to realize when the grid signals generate waveform distortion, even if the system adopts the digital phase-locked frequency multiplier technology[5]. In addition, the two technologies, windowing technology and windowing-interpolation technology, need amounts of real-time calculations, and the selected window function has a great influence on the analytical results. This makes FFT difficult to obtain higher harmonic measurement results when the system is in the process of spectral analysis[9].

Fast Anti-aliasing Fourier Transform Algorithm FAFT, can not only suppress the spectrum aliasing error in the case of not filtering the signal of high-frequency component, but free of the limit of applied constant force. This can be analyzed to figure out higher than N / 2 (N is the sampling points of one cycle) harmonic component. Obviously, this algorithm can not only simplify the hardware structure, spread spectral analysis range, but also improve the accuracy of spectral analysis and calculation speed, which is an effective calculation method.

For the periodic signal x(t), the period is T and the time interval is Δ, which carry out period sampling, the total sampled points are N+1(N is an even number), T=NΔ. Suppose that the rth point's sampled value is x_r（r=0，1，2,．．．,N), then the basic formula of the FAFT algorithm is shown as follows[10]:

$$\dot{A}_k = 2u_k \dot{A}_{even}(k) + R_k \dot{A}_{odd}(k) W_N^k - Z_k F \qquad (1)$$

in the formula：

$\dot{A}_{even}(k)$ and $\dot{A}_{odd}(k)$ are respectively signal's even sequence and odd sequence of Fourier transform, the specific calculation formula is shown as follows:

$$\dot{A}_{even}(k) = \sum_{r=0}^{\frac{N}{2}-1} \left(\frac{x_{2r}}{N} W_N^{2rk}\right) \qquad (2)$$

$$\dot{A}_{odd}(k) = \sum_{r=0}^{\frac{N}{2}-1} \left(\frac{x_{2r+1}}{N} W_N^{2rk}\right) \qquad (3)$$

From the formula（1）to（3）, $W_N = e^{-j\cdot\frac{2\pi}{N}}$, $F = x_0 - x_N$, coefficients u_k、R_k、Z_k, are just relevant with K and N. In addition, according to the cycle recursive properties of $\dot{A}_{even}(k)$, $\dot{A}_{odd}(k)$ and W_N^k, recursion algorithm of formula (1) is worked out:

$$\dot{A}_{k+mN} = 2u_{k+mN} \dot{A}_{even}(k) + R_{k+mN} \dot{A}_{odd}(k) W_N^k - Z_{k+mN} F \qquad (4)$$

$$\dot{A}_{k+(m+\frac{1}{2})N} = 2u_{k+(m+\frac{1}{2})N} \dot{A}_{even}(k) + R_{k+(m+\frac{1}{2})N} \dot{A}_{odd}(k) W_N^k - Z_{k+(m+\frac{1}{2})N} F \qquad (5)$$

According to the formulas(1)-(5),using the signal sampling data, we can calculate each harmonic data of the grid signals quickly and efficiently. By contrasting the experiments, we found that the analysis accuracy of FAFT is a lot higher than FFT, especially when the sampling points are N / 2 times or more, the results of FFT has presented great error, so it has little value in use, but FAFT can still maintain the analysis accuracy like the case when the sampling points are below N/2.

4. Software Design

The system software design is mainly divided into two parts.

(1). Quartus II and DSP Builder are used to complete the construction of the NiosII system.

(2). Nios II IDE is used to complete the compiling of the system control and algorithm. Using the modular design method, monitor software mainly completes system initialization and hardware self-checking cycling, FAFT processing of the sampled voltage and current data, operation processing of voltage, current, power, etc, key processing, display and saving the results. The flow diagram of the system software design is shown in Figure 3.

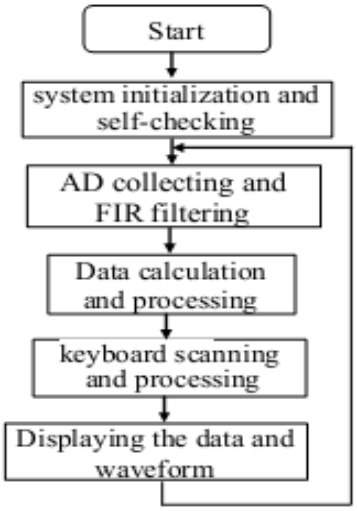

Fig. 3: software flow diagram

5. Conclusion

The power quality analysis system is designed to realize the network multi-parameter measurement, with taking advantages of SOPC technology. The hardware description language is used to achieve A/D controlling, realize digital phase-locked frequency multiplier circuit and data synchronously sampling, which has good portability and scalability, and even more, so debugging and modifying is facile. Moreover, the FAFT algorithm applied in the software ensures the measurement accuracy of the higher harmonic content rate. All in all, the system realizes the high integration and reliability.

6. Acknowledgments

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7. References

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