# CMOS Design And Single Supply Level Shifter Using 90nm Technology

**Shilpa Thakur**
*ME Student*
*NITTTR, Chandigarh India*
*Shilpa.thakur75@gmail.com*

**Rajesh Mehra**
*Associate Professor*
*NITTTR, Chandigarh , India*

## Abstract

The design and application of level shifter circuit which is based on single power supply is presented in this paper different from conventional level shifter circuitry. A level shifter may be used to shift any voltage level to a desired level without any leakage current. To reduce the supply routing and layout congestion within the chip whenever level shifting is needed for different voltage it decreases pin count also. In multi voltage system a level shifting is required for two or more chips which are operating at different supply voltage. The circuit of level shifter is generic in nature and voltage level shifting done is restricted by technology. 90 comes nm technology is used to design the circuitry which is simulated in SPICE (simulation program with integrated circuit emphasis). Simulation result of this level shifter circuit is capable to shift input voltage from 1.5V to 3.00V at frequency of 1GHZ.

*Keywords:* Conventional level shifter, Low power, Single supply level shifter circuit Description

## 1 .Introduction

VLSI technology is a technology by which we can design complex system on chip where all elements of system like analog and digital circuit, passive element are integrated on single chip. These different elements of chip run at different –different voltages to get required speed and power. Chip having different supply voltage for the communication among the different elements of chip[1-4], so level shifters are used to convert logical signal from one voltage to another voltage. Apart from this level shifters are used at the pad ring and core of chip interface where low voltage signal from chip core are shifted to high voltage [4-6]. Proposed level shifter and conventional level shifters use two voltage supplies, input voltage supply (Vdd) and output voltage supply (Vod). Schematic diagram of conventional level shifter is shown in figure 1. I/P supply voltage (Vdd) and output supply voltage (Vod) are used.

 

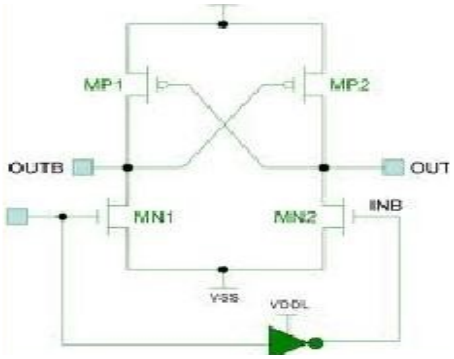


Fig. 1 conventional Level shifter

## 2. Single Supply Level Shifter

The main purpose of designing of schematic diagram of single supply level shifter is to extract lower level from input signal will be high Vddh now MN2 is turned ON and OUT B is pulled to Vss.MN1 will be get higher than Vddh and MN3 will be OFF. Therefore when input is Vddl then out will become Vddh .[7-10] When input will be at logic low Vss first of all Vc will be at Vddl which make the MN3 turned ON.MP3 is weak as compared to MN3. To maintain Vc. So that it become discharge prior to OUT. Choosing the size of MN3 and MP3 is important during designing and it is dependent on frequency of operator when gate is at Vdd MN1 get turned OFF and MN2 get turned ON. Here output of level shifter OUT B and OUT will be at Vss. And Vdd at the same time MP2 will be OFF because MN1 get down OUT B to Vss due to which OUT become Vdd and Vss.

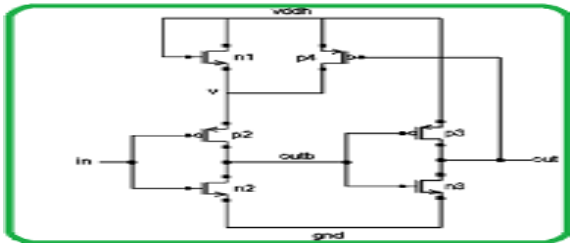


Fig.2 Proposed single supply level shifter [7]

## 3. Circuit Description and layout

The proposed single supply level shifter suffers from higher leakage current and operation is restricted with high range of input and output supplies. So schematic diagram of proposed single supply level shifter is shown in figure.4 [7-8] Single supply level shifter can be easily designed by decreasing supply voltage of inverter P2N2 by using a diode with NMOS between V and higher supply Vddh. Therefore the voltage at point V is Vddh –Vtp so that voltage at transistor N1 is Vtp where Vtp is threshold voltage. So will get turn OFF by decreasing gate to source voltage.

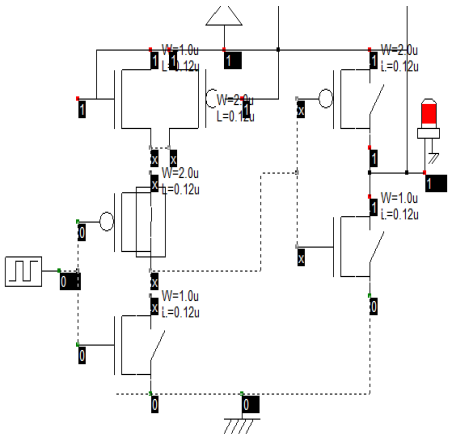


Fig.3 Single supply level shifters

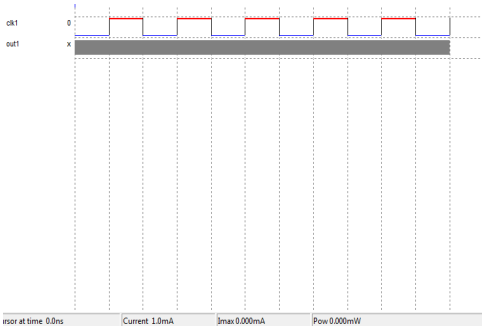


Fig.4 Timing circuit for single supply level shifter

when high input is applied. Transistor P4 get turned ON by charging point V to Vddh so supply voltage of P2N2 will be between

Vddp and Vddh will be according to the input[8-10]. When input voltage supply is low and Vddh is at higher level than input supply level greater than Vth then leakage current flow through circuit. Operating speed of circuit is restricted due to use of diode with transistor N1. It is not appropriate for low power consumption is resulted where so many level shifters are used

.

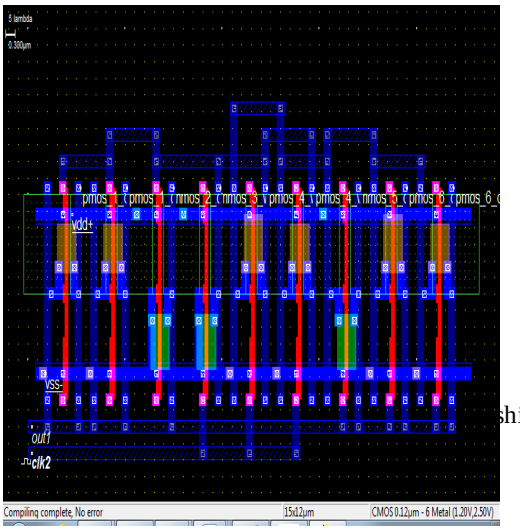


Fig.5 Layout Diagram of single supply Level Shifter

## 4. Simulation Result

Figure 5 shows simulation result of the proposed level shifter circuit which was design in 90nm CMOS process and simulated with SPICE with following parameter value.

| Vdd (volt) | Power dissipation (mW) | Max.Current |
|---|---|---|
| 1.50 | 2.0 | 1.8 |
| 2.00 | 3.8 | 3.0 |
| 2.50 | 4.9 | 3.9 |
| 3.00 | 6.0 | 5.0 |

Rise time
delay= 0.007ns
Fall time
delay=
0.003ns

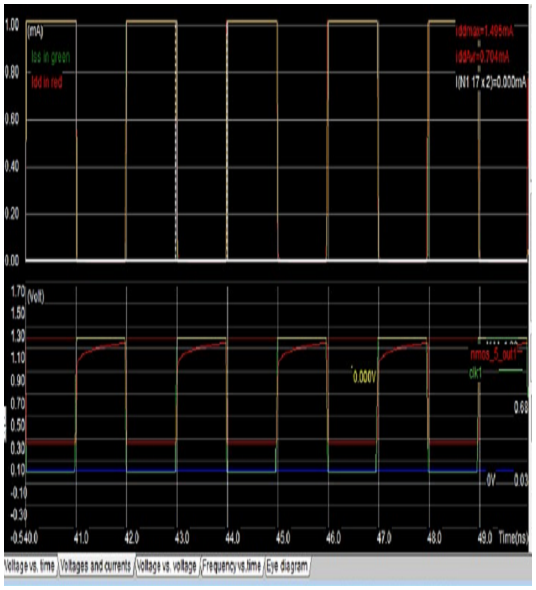

Fig.6 Simulation Result of single supply level shifter

## 5. Conclusion

Low power application can be easily carried out using single supply level shifter using single supply level shifter using zero steady state current layout complexity can be decreased by using the proposed circuit ,because only one supply is required at which shift of input logic signal is to be done. At the interface of module pin count is reduced of module which is using different level supply for level shifting. This improves overall performance of system by reducing complexity and cost of system. Shifting of lower supply signal level to higher supply signal level without consumption of steady state current is shown in simulation results


## Acknowledgements

I am greatly thankful to honorable DIRECTOR, NITTTR Chandigarh, Prof.& Head ECE Department Dr. S.B.L Sachan for their worthy guidance and help in writing this paper

**Reference:**


1. Sven Lutkemeier, Ulrich Ruckert,"A Sub threshold to AboveThreshold Level Shifter Comprising Wilson Current Mirror," in Proc. IEEE Transaction on circuit and system, vol .57,no9, Sep 2010.

2. Jianhua Ying ,Fenghu Wang ,Chuan Ding , "An Improved Negative Level Shifter for high speed ana low application" in Proc. IEEE Transaction on circuit and system,pp.1-5 Jun 2010.

3. Yan –Mang Li,Chang-Bao, Bing Yuan , "A high speed and power efficient level shifter for shifter for high voltage Buck converter driver,in Proc IEEE,Aug 2010.

4. .Philippe O .Pouloquen, "A Ratioless and biasless Static CMOS level shifter ,in Proc in IEEE ,Aug 2010.

5. A Hasanbegovic, S.Auneet , "Low power sub thresholdto above threshold level shifter in 90nnm process,"in Proc.NORCHIP Conf ,pp.1-4,Nov 2009.

6. S Maruyama, K takahashi, H Fujita, "A mems digital mirrorarray integrated with high voltage level shifter ,in proc in IEEE 2009.

7. A. Chavan, E. MacDonald, "Ultra low voltage level shifters to interface sub and upper threshold reconfigurable logiccells",in Proc. IEEE Aerosp. Conf, vo1–8, pp.1–6, Mar. 2008.

8. J. Rocha, M. Santos, J. M. Dores Costa, F. Lima, "Highvoltage tolerant level shifters and DCVSL in standard low voltage CMOS technologies," in Proc. IEEE Int. Symp. Ind. Electron, pp. 775–780, Jun. 2007.

9. T-H.Chen, J Chen, L.t.Clark, "Sub threshold to above threshold level shifter," J.Low Power Electronics, vol. 2, no.2,pp 251-258, Aug.2006.

10. E J. Mentze ,H.L Hess ,K.M.Buck, D.F Cox , "Low voltageto high voltage level shifter and related methods ,"U.S Pantent, Sep 2006

11. Bo Zhang, Liping Liang , "A new level shifter with low powerin multi voltage system, "19th International Conference on VLSI Design 2006.

12. J.C.Garcia,J.A Montiel –Nelson, S Nooshabadi , "Bootstrapped power efficient CMOS driver ,"IEEE I

13. Kyoung-Hoi Koo, Jin-Ho Seo,Myeong -Lyong Ko,Jae-Whui Kim, " A New level-up Shifter for High Speed and Wide Range Interface in Ultra Deep Sub-Micron", IEEE International Symposium , pp.1063-1065, May 2005.

14. C. Q. Tran, H. Kawaguchi, T. Sakurai, "Low–power high–speed level shifter design for block–level dynamic voltage scaling environment," International. Conference. onIntegrated. Circuit, pp. 229–232, May 2005

15. Kyoung-Hoi Koo; Jin-Ho Seo; Myeong-Lyong Ko ; Jae- Whui Kim ; "A New Level-up Shifter for High Speed and Wide Range Interface in Ultra Deep Sub-Micron", IEEEInternational symposium on Circuits and Systems, vol.2