VLSI IMPLEMENTATION OF OPTIMIZED REVERSIBLE BCD ADDER

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Abstract—Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. This paper presents an optimized reversible BCD adder using a new reversible gate. A comparative result is presented which shows that the proposed design is more optimized in terms of number of gates, number of garbage outputs and quantum cost than the existing designs.

Index Terms— Advanced computing, Reversible logic circuits, reversible logic gates, BCD adder, nanotechnology.

1 INTRODUCTION

Conventional Combinational logic circuits dissipate heat for every bit of information that is lost during their operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit if it is constructed using the reversible logic gates will allow the recovery of the information. In 1960s R. Landauer demonstrated that even with high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. It is proved that the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzman's constant and T is the absolute temperature at which the operation is performed. Later Bennett, in 1973, showed that in order to avoid KTln2 joules of energy dissipation in a circuit it must be built from reversible circuits. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Extra inputs or outputs are added so that the number of inputs is made equal to the number of outputs whenever it is necessary. An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs. Also they must use minimum number of constant inputs.

The present work proposes a BCD adder which uses a new reversible logic gate called SCL gate in combination with the existing reversible logic gates for further improvement of the optimization parameters.

The logic diagrams are given along with their logic function representations instead of the truth tables. The new reversible logic gate called SCL gate designed to get the overflow detection in BCD adder along with its logic function representation is presented.

2 BASIC REVERSIBLE LOGIC GATES

2.1 Reversible logic gate

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this bijective mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. The reversible logic circuits must be constructed under two main constraints. They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted.

2.2 Basic reversible logic gates

The important basic reversible logic gates are, Feynman gate which is the only 2*2 reversible gate which is as shown in the figure.2a and it is used most popularly by the designers for fan-out purposes.

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There is also a double Feynman gate, Peres gate, all of which can be used to realize important combinational functions and all are 3*3 reversible gates and are as shown in the figure.2b to figure.2c. The figures also show the switching functions for terminals. There are other 4*4 gates some of which are specially designed for the realization of important combinational circuit functions in addition to some basic functions.

Some of the important 4*4 gates are, TSG gate, MKG gate, HNG gat etc all of which are very useful for the construction of important reversible adders. They are also technology independent as quantum logic and optical logic and DNA logic are all still in the initial implementation stages and the technology is not defined properly. However the design methods using existing reversible logic gates and new reversible logic gates are very important and useful for building future computation circuits and also for the design of ultra low power integrated circuits. They are classified as an important theoretical computational circuits.

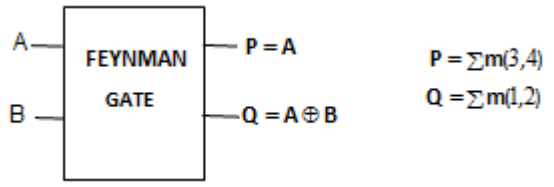


Fig.2a Feynman gate – 2*2 gate

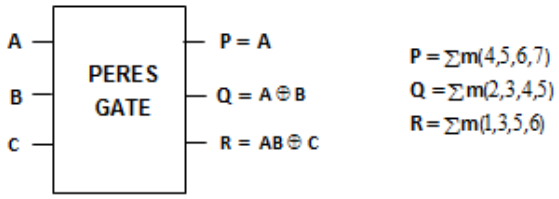


Fig.2b. Peres gate – 3 * 3 gate

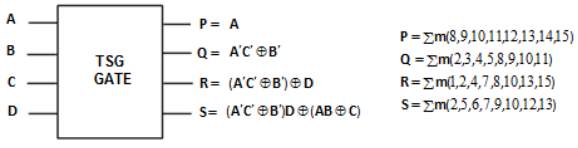


Fig.2c TSG gate – 4 * 4 gate

2.3 Optimization parameters

The important parameters which play a major role in the design of an optimized reversible logic circuit are,

- *Constants:* This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- *Garbages:* This refers to the number of outputs which are not used in the synthesis of a given function. These are very essential without which reversibility cannot be achieved.
- *Gate count:* The number of reversible gates used to realize the function.
- *Flexibility:* This refers to the universality of a reversible logic gate in realizing more functions.
- *Quantum cost:* This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.
- *Gate levels:* This refers to the number of levels in the circuit which are required to realize the given logic functions.

The present paper proposes one new gate, called SCL gate (Six Correction Logic) for the correction in the BCD addition and is as shown in the Fig 4.It is a 4 * 4 reversible and its logic function representation is as shown.

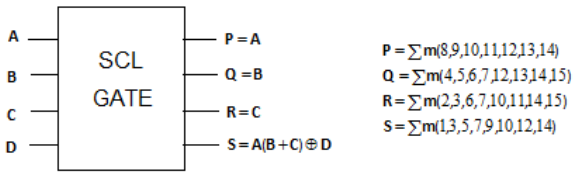


Fig.3 SCL gate –for BCD adder's six-correction logic gate.

2.4 BCD adder and the design issues

A one digit BCD adder adds two BCD numbers and produces the BCD sum after the required correction which is according to the rules for BCD addition.

III. CONSTRUCTION OF BCD ADDER

In a BCD adder, the correction logic which generates the Cout is given by,

Cout = S3S2 +S3S1+C4..... (Eq1)

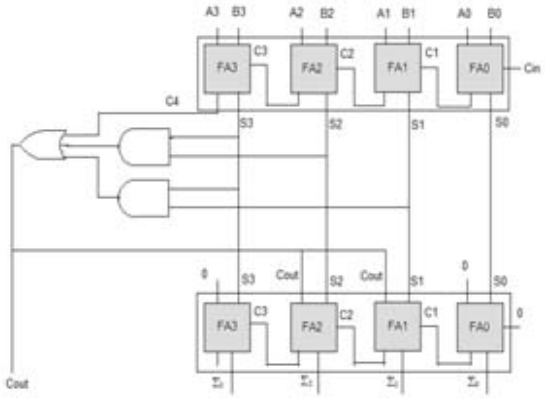


Fig. 4 Conventional 1 digit BCD adder

The above equation can also be expressed without changing its functionality into,

Cout = C4⍰S3 (S2+S1)..... (Eq2)

The BCD adder can be constructed using reversible gates. Fig5 shows the 4 bit parallel adder constructed using HNG gates which can also be constructed using TSG or MKG gates.

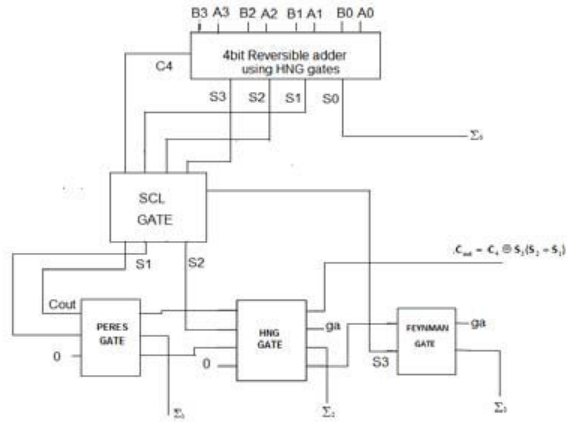
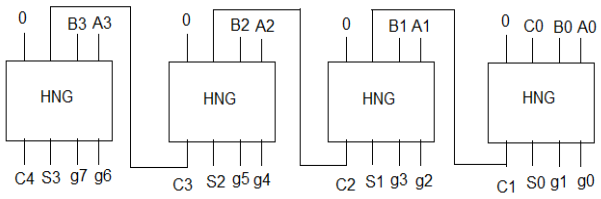


Fig. 5. Reversible implementation of a one digit BCD adder.

The proposed BCD adder circuit uses one such 4 bit parallel adder and is called as adder-1 in this proposal. The total number of garbage outputs generated from the reversible parallel adder is equal to eight. The overflow detection uses one SCL gate. This does not produce any garbage outputs. Also the second adder which should add six in order to correct and convert the sum to BCD sum need not be a 4bit parallel adder but instead it can be constructed using one Peres gate, one HNG gate and one Feynman gate similar to the existing designs.



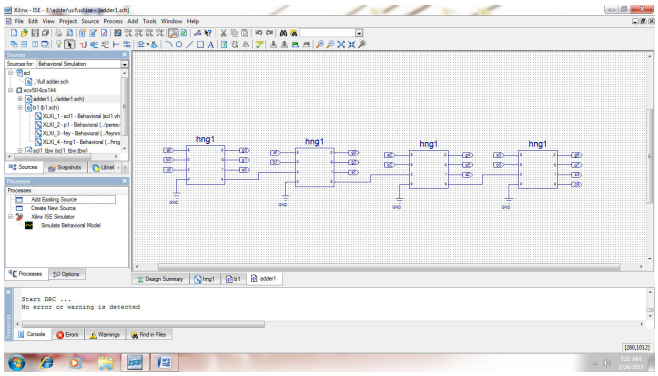
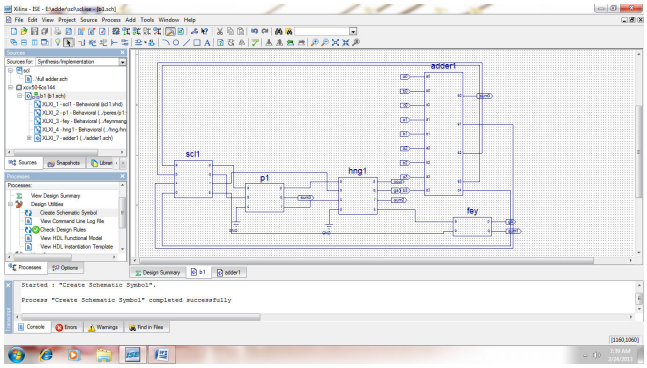


Fig.6. Used reversible 4bit parallel adder

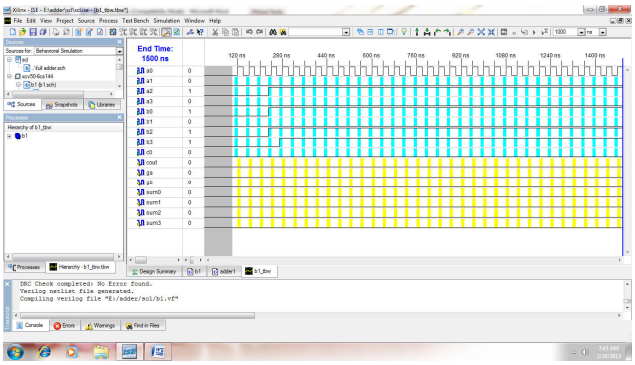


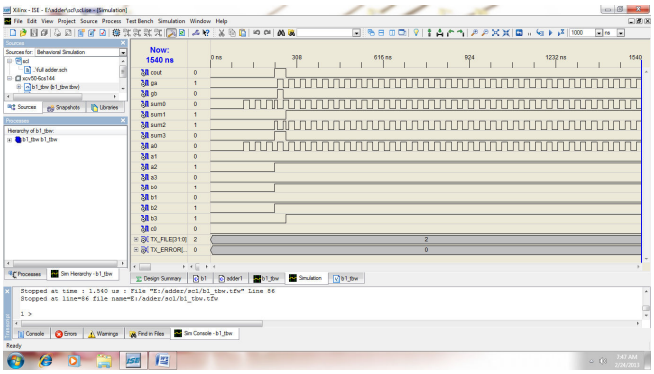
The New gate is used to add S1 with Cout to produce final ∑1 and a carry which is given to one HNG gate used as a full adder to produce final ∑2. Then the final sum bit ∑3 is obtained by using one Feynman gate. So the BCD sum is ∑3 ∑2∑1 ∑0.The complete BCD adder is as shown in the fig.6.

IV. RESULTS AND DISCUSSION

Several researchers have proposed the 4bit parallel adder which is constructed using 4*4 reversible full adder gates. It is also known that the full adder circuit requires a minimum of two garbage outputs and a constant input. This reduces the number of gates but in this paper fan-out is not taken into account which when considered will increase the number of gates above 11. This produces 22 garbage outputs with 11 constant inputs.

Simulation outputs





In the BCD adder is realized using 8 HNGs along with one HNFG and one FG for fan-outs. It also uses 2 NGs, one TG and one FG for the implementation of the correction logic. This uses a total of 14 reversible gates and it produces 22 garbage outputs with 17 constant inputs in the complete circuit.

The proposed circuit uses a total number of 8 reversible gates consisting of five HNG gates, one Peres gate, one Feynman gate and one SCL gate. Also the number of garbage outputs in the proposed design is 10 which is once again less as compared to that of the designs presented in.

The total delay of the BCD adder is calculated in terms of the gate delays. If the delay taken to produce the final BCD sum is ηsum then for a single BCD adder block the total delay is given by,

ηsum= ηadder1 + ηcorrection+ ηadder2

where ηadder1 = total delay in the 4bit reversible parallel adder.

ηcorrection = delay in generating the Cout.

ηadder2 = delay in generating the final BCD sum.

From the implementation it can be seen that

ηadder1 = 4 HNGs, ηcorrection = 1 SCLG

ηadder2 = 1PG + 1 HNG + 1 FG.

Therefore ηSum = 8 gate delays.

V. CONCLUSIONS AND FUTURE WORK

In this paper an optimized reversible BCD adder is presented. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers. It is shown that the proposal is highly optimized in terms of number of reversible logic gates, number of garbage outputs and the delay involved.
This delay is useful in calculating the delay involved in an N-digit BCD adder. The delays involved in the other papers are calculated on the similar lines.

The analyses of various implementations discussed are tabulated in Table-1.It gives the comparisons of the different designs in terms of the important design parameters like number of reversible gates, number of garbage outputs, and number of constant inputs in addition to the delay parameter. From the table it is observed that the present proposal uses least number of gates producing least number of garbage outputs and has the minimum gate delay compared to the other design methods.
Because of these optimization parameters the overall cost of the circuit will be reduced. The design method definitely useful for the construction of future

computer and other computational structures. Alternate optimization methods are under investigation as a future work.

Table 1 comparative analysis of various bcd adder implementations

Reversible BCD adder	Adder-1		Correction circuit + Fan-out		Adder-2		Complete circuit			Total delay to generate the sum in terms of number of gates
	No. of gates	No. of garbage outputs	No. of gates	No. of garbage outputs	No. of gates	No. of garbage outputs	No. of gates	No. of garbage outputs	No. of constant inputs	
BCD adder[13] With out Fan-out	4	8	3	6	4	8	11	22	11	10
BCD adder[14]	4	8	3+3	6	4	8	14	22	17	13
BCD adder[15]	8	8	7	6	8	8	23	22	17	14
BCD adder[16]	4	8	3	1	3	2	10	11	7	10
BCD adder[17]	4	8	2	1	3	2	9	11	7	9
Proposed BCD adder	4	8	1	0	3	2	8	10	6	8

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