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Simulation and Analysis of Controllers of DSTATCOM for Power Quality Improvement

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Abstract: Power quality is an issue that is becoming increasingly important to electricity consumers at all levels of usage. Sensitive power electronic equipment and non-linear loads are widely used in industrial, commercial and domestic applications leading to distortion in voltage and current waveforms. The widespread use of electronic equipment, such as information technology equipment, power electronics based drives such as adjustable speed drives (ASD), programmable logic controllers (PLC), energy-efficient lighting, led to a complete change of electric loads nature. These loads are simultaneously the major causes and major victims of Power Quality (PQ) problems. Voltage Sag/ Swell, Interruptions, Flickers, Harmonic distortion and Poor power factor are the main problems those are associated with power quality. For mitigating the PQ problems various measures have been developed, in this paper a comparative study has been done for controllers of the SATCOM with linear as well as non- linear loads. SRF (Synchronous Reference Frame Theory), IRPT (Instantaneous Reactive Power Theory) and PI controller based Theory have been used for generating the reference source currents. This paper presents power quality improvement in the form of Power Factor Correction, Harmonic reduction and reactive power compensation using DSTATCOM and simultaneously Simulink models which are based on the Voltage Source Converter (VSC) principle have been developed. The DSTATCOM injects a current into the system to mitigate the problems associated with power quality specially in the case of load unbalancing. Results are shown in the form of waveforms using MATLAB. The simulation is performed in MATLAB in SIMULINK environment and PSB toolboxes have been used.

Keywords- DSTATCOM, CPD's, Voltage Sag/swell, Voltage Source Converter (VSC), PCC, power quality.

I. INTRODUCTION

The area of Power Quality Issues and Remedial Measures has received considerable attention from the power utilities, power consumers and power equipment manufacturers over the last decade. Large-scale use of bulk power Thyristor Converters and industrial electronic equipment resulted in waveform pollution at all levels in the power systems from mid-eighties onwards. The issue became more serious with the proliferation of non-linear loads (rectifiers, arc furnaces, variable speed drives, UPS, computer load, printers, domestic electronic equipment etc.) in the industrial, commercial and residential sectors in the past decade. These loads, as a rule, draw non sinusoidal currents from the supply and lead to voltage distortion at the point of common coupling (PCC) and this affects the other neighboring loads those are connected to the same system and cause of poor Power Quality. With the advancement many mitigating devices are being developed, e.g. DSTATCOM, DVR and UPQC. DSTATCOM (Distribution Static Compensator) is a kind of custom power device connected in shunt with load [1-3]. The performance of DSTATCOM depends upon the control algorithm[8-20] used for the generation of reference source currents. For this many control theories are reported in literature, and some of these are Instantaneous Reactive Power (IRP) theory, Synchronous Reference Frame (SRF) theory, PI controller based algorithm, Symmetrical Component theory, and scheme based on neural network techniques [8-20]. In this paper an effort has been done for performance analysis of DSTATCOM in different control algorithms. A MATLAB- based simulation study is presented for various control algorithms of DSTATCOM. The performance of DSTATCOM is analyzed with linear as well as non linear load. Simulation results demonstrate the effectiveness of controller of DSTATCOM for reactive power

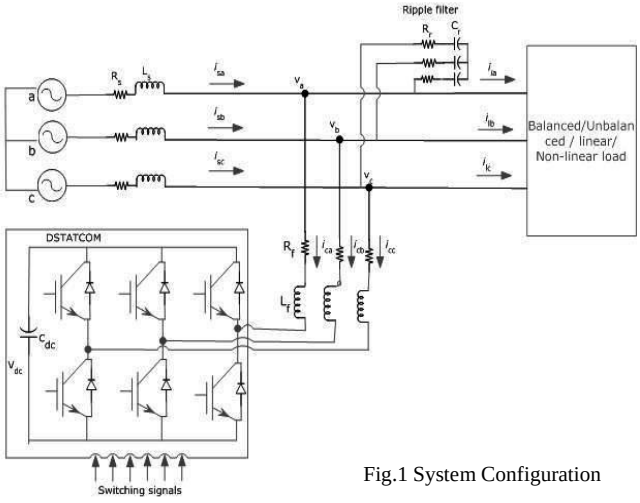

Fig.1 System Configuration

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compensation, harmonic reduction and load balancing under the unbalanced conditions.

II. SYSTEM CONFIGURATION

Fig. 1 shows the basic circuit diagram of a DSTATCOM system with balanced/unbalanced, linear or non-linear loads connected to a three-phase three-wire distribution system. The VSC used in a DSTATCOM is a type 1 converter with PWM control over the magnitude of injected AC voltage while maintaining a constant DC voltage across the DC capacitor. Fast switching power semiconductor devices such as IGBT are used instead of Thyristor or GTO Thyristor. The rapid switching capability provided by IGBT enables the use of more sophisticated control scheme to provide functions of balancing of current and voltage regulation.

A DSTATCOM can be viewed as a variable current source determined by the control algorithm. Lagging power factor load is realized by star connected resistive-inductive load. An unbalancing is realized by disconnecting load from phase c using circuit breaker model of power system. At ac side, the interfacing inductors are used to filter high-frequency components of compensating currents. DSTATCOM has no energy storage component except an electrolytic capacitor (C_{dc}) at its dc link. The system parameters viz. system voltage, series impedance, DC link voltage and load impedance are indicated in Appendix.

III. CONTROL ALGORITHMS

1. SRF(Synchronous Reference Frame) Theory: The SRF control theory [2] is based on the transformation of currents in synchronously rotating *d-q* frame Fig.2 shows the basic block diagram[2],[3] of this theory. The desired source currents in d-q frame are obtained as:

$$i_{sd}^{*} = i_{Lddc} + i_{cd} \quad (1)$$

$$i_{sq}^{*} = i_{Lqdc} + i_{cq} \quad (2)$$

where i_{sd}^{*} and i_{sq}^{*} are estimated dc components of active and reactive current component of reference Source currents in d-q frame. i_{Lddc} and i_{Lqdc} are the DC components corresponding to the load active and reactive powers and i_{cd} and i_{cq} are PI controller outputs corresponding to required current for self supporting DC bus and voltage regulation at PCC as:

$$i_{cd} = K_{pd}V_{dce} + K_{id}\int V_{dce}dt \quad (3)$$

$$i_{cq} = K_{pa}V_{e} + K_{ia}\int V_{e}dt \quad (4)$$

where $V_{dce} = V_{dc}^{*} - V_{dc}$ = error in DC bus voltage. V_{dc}^{*} and V_{dc} are the reference voltage and actual voltage of DC bus of DSTATCOM respectively. K_{pd} and K_{id} are the proportional and integral gains of the PI controller over the DC bus voltage of DSTATCOM and $V_e = V_t^{*} - V_t$ = error in amplitude of the PCC voltage. V_t^{*} and V_t are the reference voltage at PCC and amplitude of PCC voltage respectively. K_{pa} and K_{ia} are the proportional and integral gains of the PI controller over the PCC voltage.

The d-q component of the load currents are computed from the following equations:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = 2/3 \begin{bmatrix} \sin\omega t & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (5)$$

The average value of i_{ld} and i_{lq} are obtained from the two identical low pass filters i_{lddc} and i_{lqdc}. i_{cd} and i_{cq} are the outputs of the DC voltage PI controller and AC voltage PI controller respectively. The reference source currents are achieved as:

$$\begin{bmatrix} i^{*}_{sa} \\ i^{*}_{sb} \\ i^{*}_{sc} \end{bmatrix} = 2/3 \begin{bmatrix} \sin\omega t & \cos\omega t \\ \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i^{*}_{sd} \\ i^{*}_{sq} \end{bmatrix} \quad (6)$$

where the signals sinωt and cosωt are obtained using the PLL over PCC voltage. For the power factor correction mode, i_{sq}*= reactive power to regulate the PCC has some definite value depending upon the load reactive power and required reactive power to regulate the voltage at PCC estimated by the PI controller which must flow in the source and to be supplied by DSTATCOM. The extracted reference source currents (i_{sa}*, i_{sb}* and i_{sc}*) are compared to sensed source currents (i_{sa}, i_{sb} and i_{sc}) to generate the gating signals for the DSTATCOM.

2. IRP (Instantaneous Reactive Power) Theory:

In this control scheme[2,15], as shown in Fig. 3, first the sensed PCC voltages and the sensed load currents both are converted in α-β frame using the Clark's transformation as:

$$\begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (7)$$

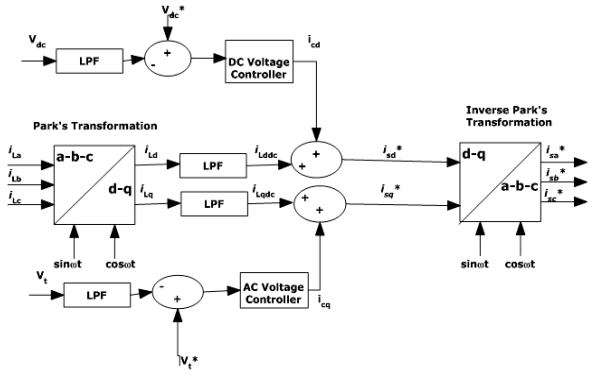

Fig. 2 Block diagram of SRF control

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \sqrt{2/3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (8)$$

The PCC voltages and load currents in α-β frame are used to calculate the instantaneous load active and reactive powers which have two components first one DC component and second one AC component and it can be expressed as:

$$p = v_a i_{La} + v_b i_{Lb} + v_c i_{Lc} = v_\alpha i_{L\alpha} + v_\beta i_{L\beta} = p_{dc} + p_{ac}$$

$$q = 1/\sqrt{3}\{i_{La}(v_c - v_b) + i_{Lb}(v_a - v_c) + i_{Lc}(v_b - v_c)\} \quad (9)$$

$$= v_\alpha i_{L\beta} - v_\beta i_{L\alpha} = q_{dc} + q_{ac}$$

For extracting the DC component of the load powers, a set of low pass filter is used In PFC mode DC voltage controller is used for maintaining the constant DC bus Voltage. In the PFC mode, only the DC component of the load active power and the DSTATCOM losses must be supplied by the source. Thus, for extracting the reference source current in PFC mode, the estimated source power can be given as:

$$p^* = p_{dc} + p_{loss};\ q^* = 0 \quad (10)$$

In ZVR mode of the DSTATCOM, an extra reactive power in addition to the load reactive power is supplied by the DSTATCOM to compensate the voltage drop in the source impedance and the active power is supplied by the source. Thus resulting source currents become leading -for the lagging and UPF loads. Therefore, in this case the reference source currents are generated by using the DC component of the load active and reactive powers along with the output of PI voltage controllers at DC bus of DSTATCOM and at PCC voltage. The estimated power for extracting the reference source currents can be given as:

$$p^* = p_{dc} + p_{loss};\ q^* = q_{VR} - q_{dc} \quad (11)$$

where q_{dc} is the DC component of the load reactive power and q_{VR} is the required reactive power for the voltage regulation at PCC and this is estimated by the PI controller over the PCC voltage as:

$$q_{VR} = K_{pa} V_e + K_{ia} \int V_e dt \quad (12)$$

where $V_e = V_t^* - V_t$ = error in amplitude of the PCC voltage. V_t^* and V_t are the reference PCC voltage and amplitude of PCC voltage respectively. K_{pa} and K_{ia} are the proportional and integral gains of the PI controller over the PCC voltage. The amplitude of PCC voltage can be calculated as:

$$V_t = \sqrt{((2/3)(v_a^2 + v_b^2 + v_c^2)} \quad (13)$$

The estimated power is used to obtain the currents in α-β frame for extracting the reference source currents as:

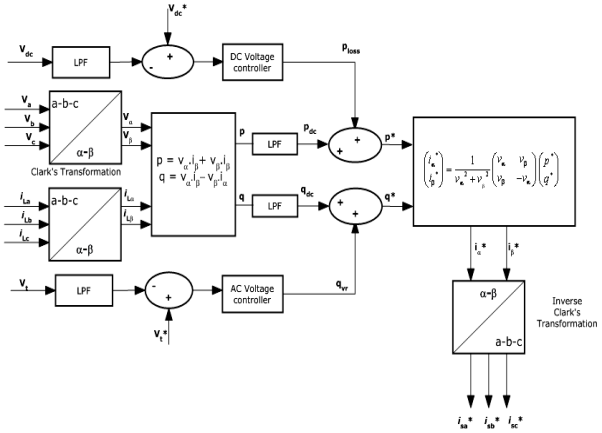

Fig.3 Block diagram of IRPT control

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2}\begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix}\begin{bmatrix} p^* \\ q^* \end{bmatrix} \quad (14)$$

Then these source currents in α-β frame are transformed in three phase using inverse clark's transformation as:

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \sqrt{2/3}\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix} \quad (15)$$

These extracted reference source currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) and the respective sensed source currents (i_{sa}, i_{sb} and i_{sc}) are used in PWM current controller to generate the switching signals for the DSTATCOM.

3 . PI controller based algorithm:

Fig.4 shows the block diagram of this control scheme [8]. In this control scheme two PI controllers are used-first one for maintaining the DC link voltage of DSTATCOM and second for regulating the amplitude of PCC voltage at load terminals. Only one PI controller is required for DC bus voltage in power factor correction, for voltage regulation both PI controllers are required. The reference source currents have two components, one in phase (I^*_{sm}) of the PCC voltage and second one is in quadrature (I^*_{sn}) with PCC voltage. To generate the reference source currents, unit templates are used which are derived from PCC voltages.

Unit templates in phase with PCC voltage are obtained as:

$$u_{sap} = v_a / V_t;\ u_{sbp} = v_b / V_t;\ u_{scp} = v_c / V_t \quad (16)$$

where V_t is the amplitude of PCC voltage.

Unit templates in quadrature with PCC voltage are obtained as:

$$u_{saq} = \left(-u_{sbp} + u_{scp} \right) / \sqrt{3} \; ;$$
$$u_{sbq} = \left(u_{sap}\sqrt{3} + u_{sbp} - u_{scp} \right) / 2\sqrt{3} \; ; \quad (17)$$
$$u_{scq} = \left(-u_{sap}\sqrt{3} + u_{sbp} - u_{scp} \right) / 2\sqrt{3} \; ;$$

The amplitude of in phase component of the reference source currents (I^*m) is computed using first PI controller over the average value of DC bus voltage (V_{dc}) of DSTATCOM and reference DC voltage (V_{dc}^*) as:

$$I_{sm}^*(n) = I_{sm}^*(n-1) + K_{pd}\{ V_{de}(n) - V_{de}(n-1)\} + K_{id}V_{de}(n) \quad (18)$$

where $V_{de}(n) = V_{dc}^* - V_{dc}(n)$ = error in DC bus voltage. K_{pd} and K_{id} are the proportional and integral gains of PI controller.

The output of this PI controller (I_{sm}^*) is used as amplitude of in-phase component of the reference source currents. Three phase in-phase components of reference source currents (i_{sap}^*, i_{sbp}^*, i_{scp}^*) are computed using unit templates as:

$$i_{sap}^* = I_{sm}^* u_{sap} \; ; \; i_{sbp}^* = I_{sm}^* u_{sbp} \; ; \; i_{scp}^* = I_{sm}^* u_{scp} \quad (19)$$

the amplitude of quadrature component of the reference source currents is calculated using a second PI controller over the amplitude of the PCC voltages (V_t) and its reference value(V_t^*):

$$I_{sn}^*(n) = I_{sn}^*(n-1) + K_{pa}\{ V_e(n) - V_e(n-1)\} + K_{ia}Ve(n) \quad (20)$$

where $V_e(n) = V_t^* - V_t(n)$ = error in amplitude of ac bus voltage. K_{pa} and K_{ia} are the proportional and integral gains of PI controller.

The quadrature components of reference source currents (i_{saq}^*, i_{sbq}^*, i_{scq}^*) are computed using unit templates as:

$$i_{saq}^* = I_{sn}^* u_{saq} \; ; \; i_{sbq}^* = I_{sn}^* u_{sbq} \; ; \; i_{scq}^* = I_{sn}^* u_{scq} \quad (21)$$

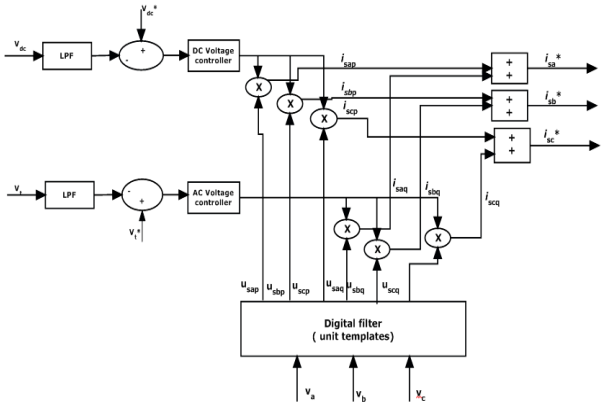

Fig.4 Block diagram of PI controller based algorithm

total reference source currents can be calculated from in-phase and quadrature components of the reference source currents can be calculated as:

$$i_{sa}^* = i_{sap}^* + i_{saq}^* \; ; \; i_{sb}^* = i_{sbp}^* + i_{sbq}^* \; ; \; i_{sa}^* = i_{scp}^* + i_{scq}^* \quad (22)$$

These extracted reference source currents (***i_{sa}*, i_{sb}* and i_{sc}**) are compared to sensed source currents (i_{sa}, i_{sb} and i_{sc}) to generate the gating signals for the DSTATCOM.

IV. MATLAB-BASED MODEL OF DSTATCOM SYSTEM

Fig.5 shows the basic simulation model of DSTATCOM system that correlates with the system configuration shown in Fig.1 in the terms of source, load and controller. Performance of DSTATCOM is tested for 415 Volts, 50 Hz distribution system and the load is considered as 46 KW at 0.8 pf (linear) and three-phase rectifier with 26KW resistive load for non-linear. The model is assembled using SIMULINK blocks. The simulation is carried out with ode 45s (Dormand-prince) variable solver with 50µsec sampling time.

V. RESULTS AND DISCUSSION

1. *SRF(Synchronous Reference Frame) Theory:*

The performance of DSTATCOM is analyzed for SRF control theory in PFC as well as in ZVR mode. For creating the unbalanced condition one phase (phase-c) is opened with the help of circuit breaker model in MATLAB. The load unbalancing is done from 0.6secs. to 0.7secs for PFC mode and for ZVR mode also. Fig. 6 shows the dynamic performance of DSTATCOM in the case of linear load for PFC mode. During unbalanced load condition source currents are balanced and in phase with source voltage also so the power factor is achieved unity at the source side. With the change of load, the DC bus voltage is also regulated at its reference value of DC voltage. Fig.7 shows the dynamic performance of DSTATCOM in ZVR mode in the case of nonlinear load. All the results are same as in PFC mode and the PCC voltage is also maintained

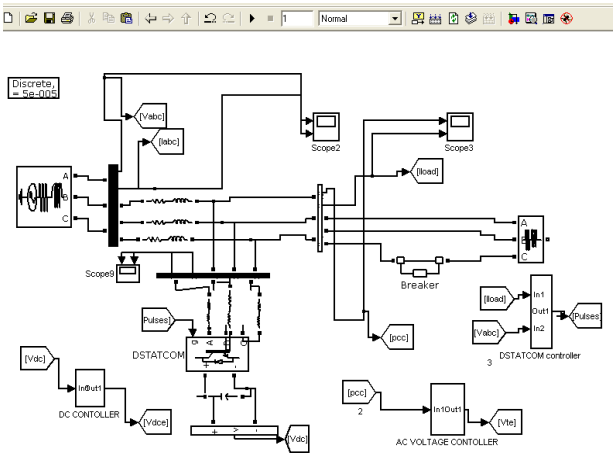

Fig.5 SIMULINK model for the test system with DSTATCOM

constant at 340 Volts (amplitude of phase voltage) during load unbalancing, thus zero voltage regulation is achieved at PCC and the DSTATCOM works in ZVR mode. % THD in source current is calculated as 3.42% while in the load current %THD is 23.52%. So the harmonics are also reduced in current with SRF control algorithm.

2. IRP (Instantaneous Reactive Power) Theory:

Same results have been achieved with the IRPT for DSTATCOM. Same circuit configuration are used for this controller also. Unbalancing is also done at the same instants as in SRF algorithm. Fig. 8 shows the results in PFC mode and Fig. 9 shows the results for ZVR mode. In PFC mode power factor is achieved unity at the source side and in ZVR mode the voltage is maintained constant at its reference value at PCC. % THD is reduced upto 4% in load current that is due to nonlinear load. DC bus voltage is also regulated at its reference value.

3 . PI controller based algorithm:

Fig. 10 shows the results of PI controller based algorithm for the DSTATCOM in PFC mode and Fig. 11 shows the results in ZVR mode of operation of DSTATCOM. In PFC mode power factor is achieved unity at the source side and in ZVR mode the voltage is maintained constant at its reference value at PCC. % THD is reduced upto 4.5% in load current that is due to nonlinear load. DC bus voltage is also regulated at its reference value.

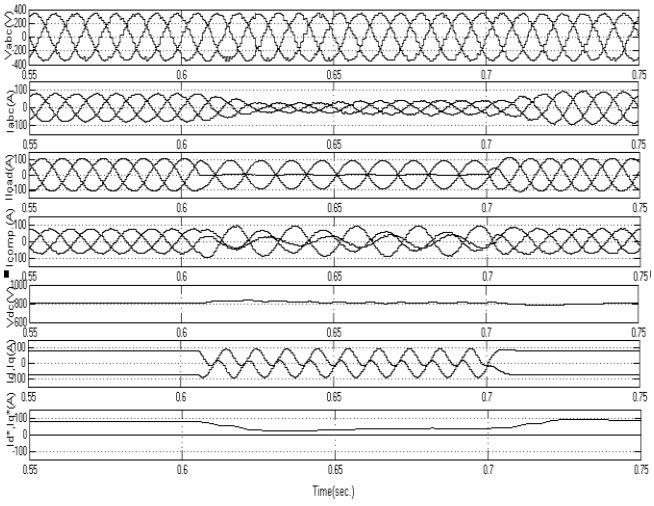

Fig. 6 Performance of DSTATCOM in PFC for linear load by SRF controller.

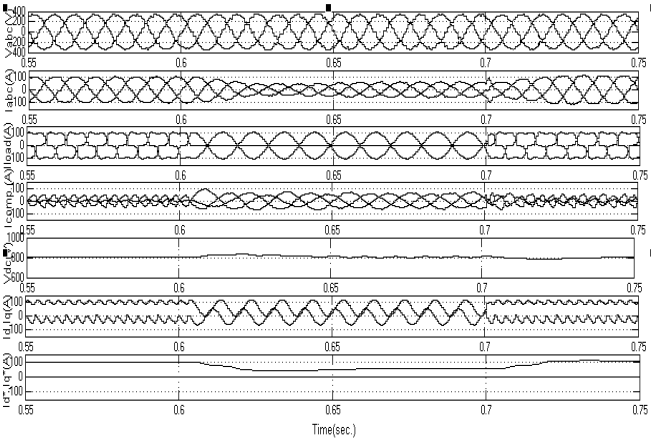

Fig.7 Performance of DSTATCOM in ZVR mode for non linear load by SRF controller.

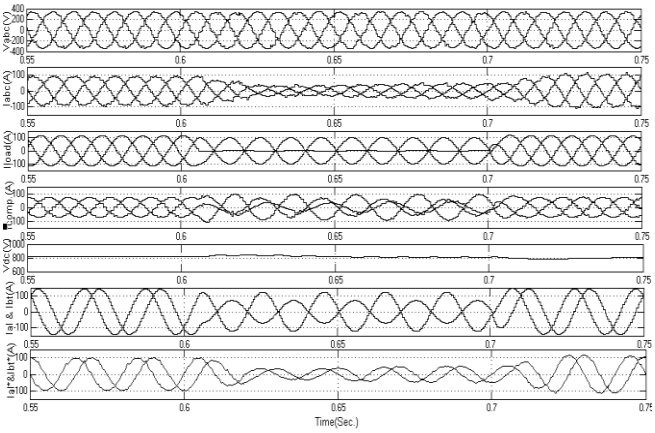

Fig.8 Performance of DSTATCOM in PFC mode for linear load by IRPT controller.

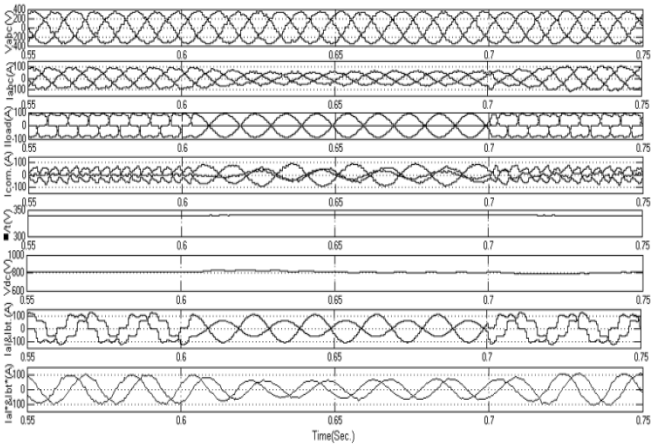

Fig.9 Performance of DSTATCOM in ZVR mode for non linear load by IRPT controller.

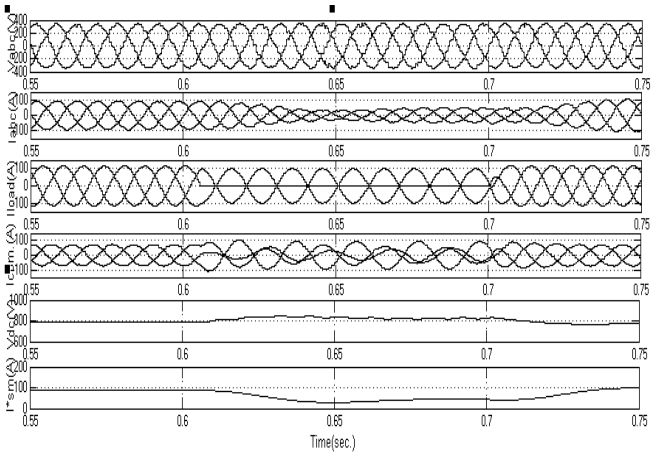

Fig.10 Performance of DSTATCOM in PFC mode for linear load by PI contoller based.

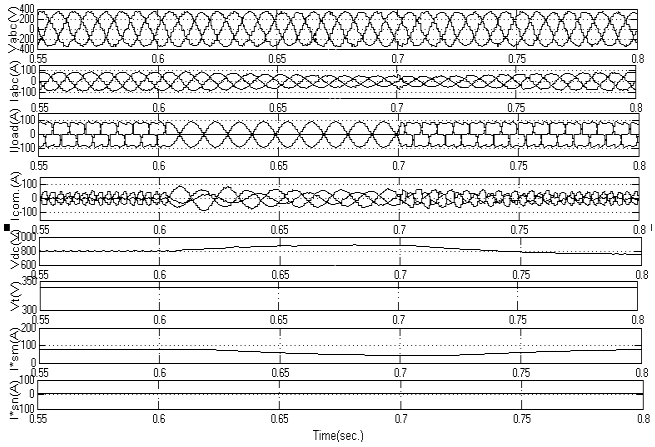

Fig.11 Performance of DSTATCOM in ZVR mode for non linear load by PI controller based algorithm.

VI. CONCLUSION

A model for DSTATCOM has been developed in the MATLAB SIMULINK environment. During load unbalancing, source currents are balanced and DSTATCOM works in power factor correction mode and zero voltage regulation mode. The results are shown in the form of waveforms for linear load as well as for non-linear load for three phase three wire distribution systems. All the results demonstrate the effectiveness of various controllers of DSTATCOM. Power Quality improvement has been achieved in terms of power factor correction, voltage regulation, DC bus voltage regulation and harmonic reduction.

APPENDIX

Source: 415 volts, 50 Hz
Source impedance: L= 0.2 mH, R = .01Ω
Load : 46KW, 0.8 pf lagging (linear), Three phase rectifier with 26KW resistive load (Non-linear load)
Switching Frequency: 10 KHz
DC bus voltage: 800 V
DC capacitor: 10000 μF
Interfacing inductor: 3.5 mH

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