Design And Optimization of Low Frequency Pushing Circuit in Voltage Controlled Oscillators

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Abstract

A low frequency pushing wide frequency tuning range Radio frequency (RF) voltage – controlled Oscillator (VCO) in 0.35 m standard CMOS prosed for wireless applications is presented. It is different from all conventional designs primarily in the way it is biased. The measurement results show that the proposed structure reduced the frequency pushing to 0.55 % /V and increase the frequency tuning range to 526 MHz It provides a minimum figure of merit for oscillators (FOM) of about – 180.7dBc/Hz following the optimization method. The main contributions include:
(a)the proposed VCO structure, (b) the FOM optimization method and (c) the silicon results.

KEYWORDS: VCO, Frequency pushing, Wide Tuning Range, Figure of merit, Phase noise

1. INTRODUCTION

The low phase noise and low power voltage - controlled oscillator (VCO) play a very important role in Radio frequency (RF) transceivers and has attracted much research effort recently, See Refs. 1 – 9. In most VCO designs, optimization on phase noise and power consumption is necessary in reaching the best trade – off for a give application. Wide frequency tuning range is another important topic in VCO design,See Refs.1, 2. Enlarging the turning range is demanded not only for combating unexpected large process variation in on – chip LC – tank, but also for multi – band applications. Besides, in VCO design, low frequency pushing become stringent requirement due to limitations and variations in the power supply particularly when the supply is shared among blocks working at different frequencies, e.g. in single – chip transceiver implementations.

Most of the existing VCO designs are mainly based on the NMOS – PMOS cross – coupled pair complementary structure.See Refs. 2, 3, 4 or "(1) NMOS cross –coupled" . The complementary structure usually consumes less power for a given phase noise because its amplitude is twice than that of the NMOS pair structure. But the latter one can provide wider frequency tuning range for equal loop transconductance. Unfortunately, in these two structures, NMOS transistors located in the cross-coupled pair and tail current source degrade the phase noise much at small offset frequency, such as 100kHz, due to their higher flicker noise coefficient than that of PMOS transistor Refs. 5. Moreover, the simulation results Refs.6, 7. show that both structures suffer from poor frequency pushing performance.

In this paper, we propose a VCO structure that is based on low Q LC-tank and features very low frequency pushing and wide frequency tuning range. Its phase noise and power consumption is optimized using FOM method as described in Section III. The circuit is optimized and implemented using 0.35µm standard CMOS process.

The proposed VCO structure is presented in Section II. In Section III, its design and optimization procedure are discussed. Experimental results are provided in Section IV. Conclusions are drawn in the last section.

2. PROPOSED VCO STRUCTURE

Fig.1 shows the proposed structure of differential CMOS LC-tank VCO where two-transistor biasing technique Refs. 6, is applied. It has one VCO-core and two buffers with differential outputs taken from OSC_A and OSC_B. The VCO-core can be divided into three main parts: LC-tank, negative Gm generator and bias circuit. The LC-tank is built with two spiral inductors and two accumulation-mode MOS varactors. The capacitances of MOS varactors are adjusted by varying the potential of separated N-well through control voltage Vctrl. Two cross-coupled PMOS transistors MP1 and MP2 are used as the negative Gm generator to compensate the loss in the LC-tank during the oscillation.

The PMOS type VCO-core has three main advantages:

1) Comparing with the complementary structure, the number of the transistors in the oscillation loop, which are the main phase noise contributors, is reduced from four to two.

2) According to noise models in Refs. 8, PMOS transistor inherently has lower flicker noise coefficient than NMOS transistor, especially for short channel devices. The all-PMOS type negative Gm generator leads to alower phase noise at small offset frequencies, such as 100 kHz.

3) The circuit is compatible to the N-well CMOS process, thus, enabling each PMOS transistor to have its own N-well to avoid the body effect, which is usually a problem for NMOS transistors in cascade structures.

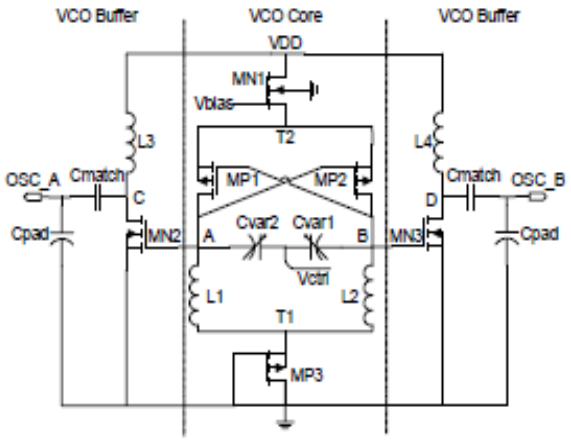

Fig.1. Proposed VCO Structure

The two – transistor biasing technique includes the bottom tail PMOS transistorMP3 and the top tail transistor MN1. Self-biased transistor MP3 is primarily used to set DC voltage of the gate of MOS varactors in order to have benefit of the full tuning capability of the accumulation-mode MOS varactors. In conventional structures, using the full tuning capability of MOS varactors has been a limitation. This provides improvement over the prior structures in three ways Refs. 6. Firstly, it extends the tuning range based on the near-zero centered capacitance tuning characteristics of accumulation-mode MOS varactor; secondly, it eliminates the need of negative voltage reference that is lacking in most wireless systems; lastly, it contributes to the improvement on frequency pushing performance. The transistor MN1, operated in the saturation region, offers a simple solution to suppress the noise from power supply, thus leads to a better frequency pushing performance, without much degradation in the phase noise. This NMOS transistor is a good choice to lower

frequency pushing although it brings a significant body effect and requires additional voltage headroom.

3. CIRCUIT DESIGN AND OPTIMIZATION

The design flow is divided into two main steps, i.e. initial design followed by the optimization. The initial design starts with an ideal LC-tank with a highest ratio of L/C for the maximum Q factor of the LC-tank, Refs. 2. When one solution satisfying the basic requirements of phase noise, power consumption and frequency tuning range with a safe oscillation start-up comes out, it can be used as a seed of the trade-off circle in the optimization part. In this most time consuming step, a design with the best FOM can be found bytuning the sizes of spiral inductors, MOS varactors, transistors and tail current. A few rules of thumb observed while optimizing the FOM are depicted in Fig.2, Refs. 7.

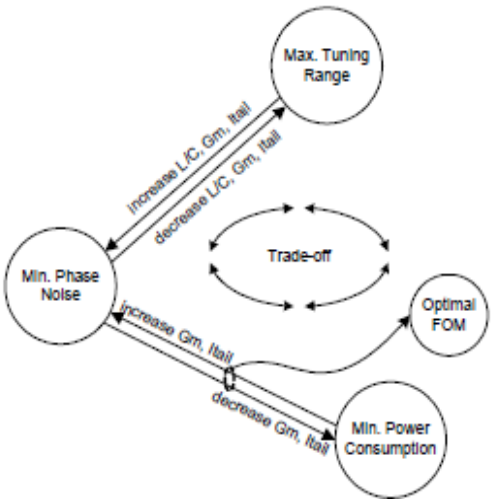

Fig.2. FOM Optimization Guideline

The widely used FOM is calculated by

$$\mathbf{FOM = L\{\Delta\omega\}(\Delta f/f_0)^2 PVCO/mW} \qquad (1)$$

Where $L\{\Delta\omega\}$ is the phase noise, $\Delta f/f0$ is the ratio between the offset frequency and the carrier, and P_{VCO} is the power consumption of the VCO-core. Next to the initial design, the optimization of the VCO-core involves plotting the FOM curves, which is done in three steps. Step 1 is to find the minimum FOM point at a starting tail current by finely tuning the sizes of MOS transistors in the VCO-core, e.g. -180.3dBc/Hz in the FOM curve at 2.5mA tail current. In Step 2, Step 1 is repeated by varying the tail current, from 1mA to 10mA in this case, to generate several sets of FOM points. Final step is to draw the curve of best FOM versus tail current as shown in Fig.3 using the minimum FOM points extracted from these FOM data sets.

In Fig.3, it is obvious that the best FOM close to -181dBc/Hz is reached at the tail current around 3.5mA. On the left of the optimized point, where the tail current decreases from 3mA, the VCO-core falls into the current-limited region, Refs.4, with lower output amplitude, therefore poor phase noise and FOM. On the other side, where the tail current increase from 4mA, the VCO-core goes into the deep voltage-limited region Refs.4, in which the phase noise does not run as fast as the increase in power consumption, so it results in a poor FOM too.

In this design, the VCO-core tail current of 4mA is taken considering the target center frequency of 2.45GHz in the full VCO circuit. The optimal sizes of MOS transistors in the VCO-core are determined by the data gathered during the step 1 and step 2 of FOM optimization method.

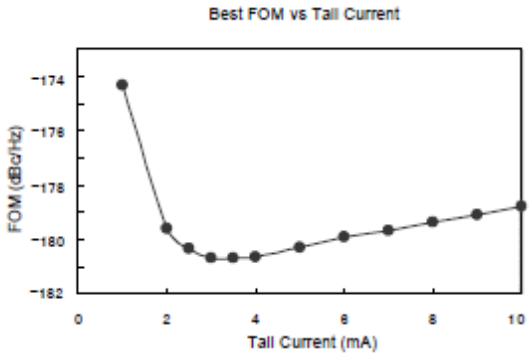

Fig.3. Plot of best FOM Versus Tail Current

The NMOS type single-stage VCO buffer is also shown in Fig.1. The VCO buffer isolates the inner core from outer circuits while providing impedance match to 50Ω. The optimization of sizes of MN2 (or MN3), L3 (or L4) and Cmatch are required for the best impedance match. Metal Insulator Metal (MIM) structure is used for realizing the capacitor Cmatch in this matching network as it provides high quality factor, high self-resonance frequency, exceptional linearity and small bottom-plate capacitance although it is typically less area efficient than other types of capacitor structures.

4. EXPERIMENT RESULTS

The proposed design is fabricated using 0.35µm standard CMOS process. Fig. 4 shows the die-microphotograph. The required silicon estate excluding pads is about 0.2mm2 only. The experiment results show that the center frequency and frequency tuning range of the proposed design are 2.278GHz and 22.6% (526MHz), respectively (Fig.5). It has a tuning sensitivity of about 258MHz/V. The wide tuning range covers a frequency range of 2.4GHz -2.48GHz for Buletooth as one of its applications. Its measured phase noise is -103.0dBc/Hz at 100 kHz offset frequency from 2.4GHz carrier (Fig.6). An output power of about 2.3dBm is noticed.

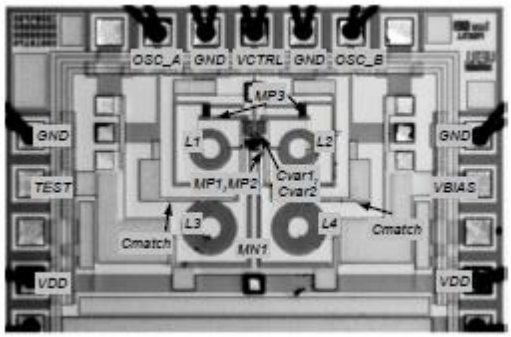

Fig.4. Die-Microphotograph of proposed VCO Design

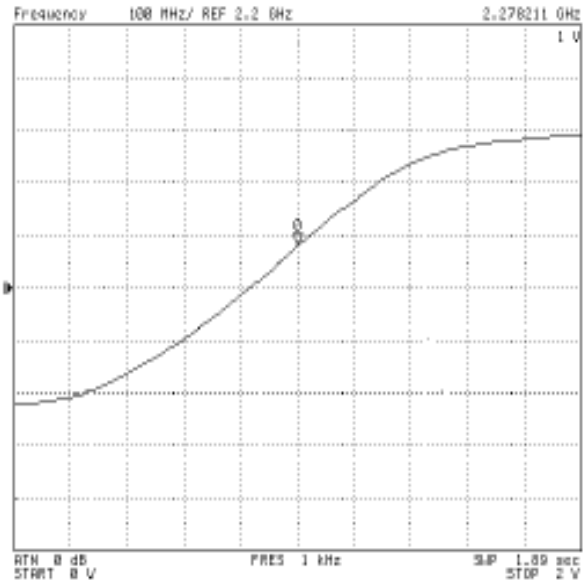

Fig.5. Measured Frequency Tuning Characteristics

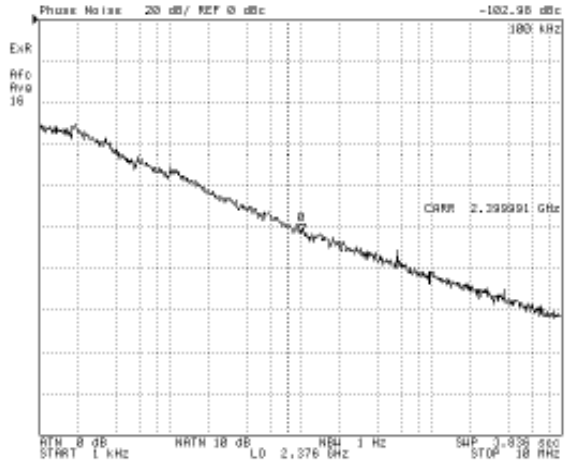

Fig.6. Measured Phase Noise at 100KHz offset frequency from 2.4 GHz Carrier

The low FOM of about -180dBc/Hz is reached in the proposed designs, thus it strengthens the fact that the proposed FOM optimization method is acceptable as an efficient approach for VCO designs. The VCO is also tested with variation in supply. We find that the proposed VCO design dramatically improves the frequency pushing to 0.55%/V, without degrading any other performances. It may be noted that the similar structure where node T1 in Fig. 1 is shorted to the ground have frequency pushing of 7.9%/V ,Refs. 6. The equation used for calculating frequency pushing is given as , Refs.6, 7:

$$\mathbf{FP = (\Delta f / f_{center}) / \Delta VDD \ \%/V} \qquad \mathbf{(2)}$$

Where f_{center} is the center frequency at normal power supply VDD, Δf is the variation of oscillation frequency due to the power supply change, ΔVDD. In Table I, the performances of different LC-tank VCO circuits reported in recent publications are compared with respect to the technology, quality factor of spiral inductor (or LC-tank), FOM, frequency tuning range and the measurement of frequency pushing. However, the published work is found lacking in reporting the frequency pushing performance.

TABLE 1
COMPARISON OF RECENTLY REPORTED CMOSLC _ TANK VCO DESIGNS.

Reference	Q	FOM (dBc/Hz)	Tuning Range	Frequency Pushing
[2], 2001	8*	-185.5	18%	N/A
[3], 2002	≈ 5.5	-180.2	14%	N/A
This work	≈ 2.5*	-180.2	22.6%	< 0.55%/V
[4], 2000	8.9	-177.8	26%	N/A
[9], 2002	6.5	-164.3	12.5%	N/A

* quality factor of the LC – tank, others are quality factor of L

This comparison shows that the proposed VCO achieves a wide tuning range and low frequency pushing with low FOM, and the overall performance of the proposed VCO design stays among the state-of-the-art in current CMOS RFIC investigations in this area.

5. CONCLUSION

An LC-tank VCO circuit has been implemented in a standard 0.35µm CMOS technology. It is based on a two-transistor biasing structure that improves the performance of frequency pushing and frequency tuning range. Final measurement of proposed structure gives 516MHz tuning range with 2.278GHz center frequency and about 0.55%/V frequency pushing in the worst case. The achieved FOM is about -180dBc/Hz, which is very close to the simulated value. This structure is proven to be particularly suitable for achieving low FOM in the VCO circuits having low Q factor LC-tank.

Both, the proposed structure and the FOM optimization method, can also be applied to the VCO designs for the applications at higher frequencies, such as 5GHz VCOs for Wireless LAN applications.

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