

Analysis and Design of Three Dimensional Free Space Optoelectronic Switching Network

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Abstract - Many research papers on optical interconnects have been published over the last three decades, however, some models are oversimplified and overlooked important design considerations. These include the timing synchronization of the VCSEL sources; detailed calculations of the free space optoelectronic interconnect network, theoretical analysis of computer generated hologram on optical interconnect system. An example of detailed analysis are presenting here for devising optoelectronic interconnect switching network based on a banyan switch. In order to expand the work into a large optoelectronic switching arrays, more careful considerations may be necessary from system perspective..

Keywords: Optoelectronic Banyan Switch, Time Synchronization, VCSEL Arrays, Temperature in Optoelectronics Interconnect.

1. Introduction

Early researches indicated that the integrated circuits have begun approaches the fundamental limits [1]. Since the electrical interconnection is treated as a uniform RLC transmission line, the coupling capacitance and on-chip inductance may cause addition delay and crosstalk, from timing diagram of electronics digital switching, because of the parasitic capacitance, voltage can not change instantaneously, in the following diagram Fig 1, this diagram defines the amount of time needed for logic signal change [2], this is called the propagation time delay t_p . We can express in the following equation [2], where this expression, the speed of logic switching depends on the value of capacitance C and the dimensions of the NMOS/PMOS transistor's width W and length L .

$$t_p \cong \frac{1.7C}{k_n \frac{W}{L} V_{DD}} \quad (1)$$

Many researchers have proposed holographic interconnections for free space interconnection; most of researches focus on Fresnel lens optical interconnects [3], other researchers proposed free space holographic interconnects [4][5][6][7]. M. Haurylau and G.Chen [8][9] indicated intra-chip optical interconnects have the potentials of outperform the electrical wires, they also perform analysis of delay as a function of interconnect width, and excellent comparison of delays, power of electrical and optical interconnects. Optical switching interconnect system time delay can be expressed in Fig 2, where in the equations, t_s stands for the rise time of optical sources, t_p represent the

response time of optical detectors, and t_e represent the response time of electronics circuits.

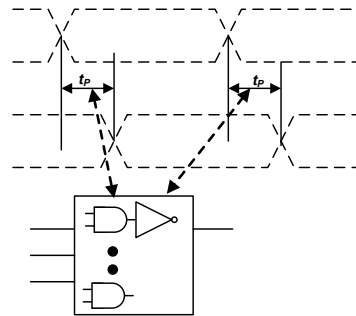


Fig. 1. Logic signal change waveform for electronics logic switching circuit

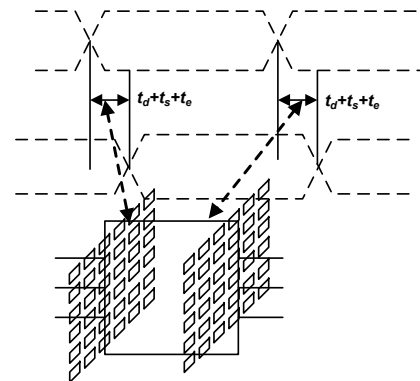


Fig 2. Logic signal change waveform for Optical Switching circuits.

2. Design Analysis of Optoelectronic Banyan Switch Network

Recent advances in high performance switching technologies [10][11] proves that Banyan switching network is one of the best choice among all different technologies. N.Andriolli [12] proposed using semiconductor optical amplifier (SOA) based photonic processing modules to implement the Banyan switching network, at earlier time. G.Li and S. Esener [13], F.E. Kiamilev [6] and G. Marsden [14] proposed similar approaches using free-space optoelectronics to implement the Banyan Switching network, however, the detailed derivations of their technical approaches were missing [4][7].

In Fig. 3 shows the architecture of optical crossbar switching interconnection network [13]. The optical crossbar

switching system forms the key components of modern optical switching network. In previous work, N.Andriolli [12] has performed preliminary design of 2x2 optoelectronic Banyan switch, each block of their optoelectronic Banyan switch is a clock driven Moore state machine. We are not going to redraw the 2x2 switching circuit here [14]; rather, the switching circuit can be shown as in Fig. 4 and Fig. 5.

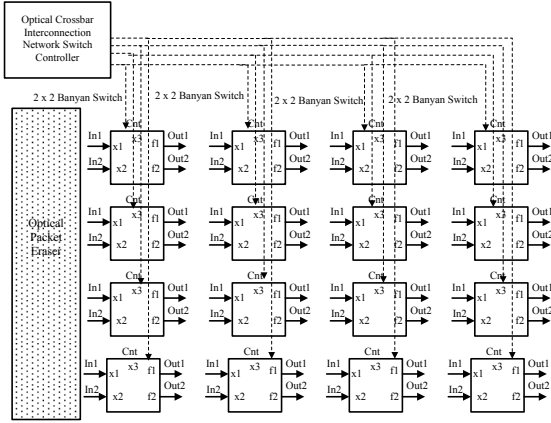


Fig 3. Architecture of an Optical Crossbar Switching Interconnection Network

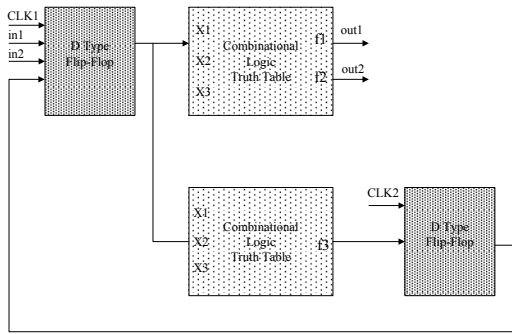


Fig 4. Architecture of 2x2 Optoelectronic Banyan Switch

X_1	X_2	X_3	f_1	$f_1(z)$	f_2	$f_2(z)$	f_3	$f_3(z)$
0	0	0	0	+1	1	-1	0	+1
0	0	1	1	-1	0	+1	0	+1
0	1	0	0	+1	1	-1	1	-1
0	1	1	1	-1	0	+1	1	-1
1	0	0	0	+1	1	-1	0	+1
1	0	1	1	-1	0	+1	0	+1
1	1	0	0	+1	1	-1	1	-1
1	1	1	1	-1	0	+1	1	-1

Fig 5. Truth Table of Combinational Logics in Fig. 4.

An optical system is a linear mapping function such as matrix multiplication, correlation or convolution of matrixes. However a truth-table mapping is a nonlinear mapping, in the earlier works [3][6], we show how to convert a nonlinear truth-table mapping into a linear relationship. Therefore, the calculations of spectral expansion matrix of above

combinatorial logic of a Banyan switch network are shown as following:

$$R = T * Z$$

$$= \frac{1}{8} \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & -1 & 1 \\ -1 & 1 & 1 \\ 1 & -1 & -1 \\ -1 & 1 & -1 \\ 1 & -1 & 1 \\ -1 & 1 & -1 \\ 1 & -1 & -1 \\ -1 & 1 & 1 \end{bmatrix}$$

$$= \frac{1}{8} \begin{bmatrix} 0 & 0 & 0 \\ 8 & -8 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} = [R_1(z) \quad R_2(z) \quad R_3(z)]$$

Fig. 6 shows the addition of two separated components of D_{++}, D_{--} and D_{+-}, D_{-+} , go through a comparator circuit to get the final truth table outputs. This comparator circuit is an improved version of the previous circuits. The inputs of the truth table go through the Boolean basis operation as shown in Fig. 7. demonstrate the simulation result of the truth-table Boolean logic switching.

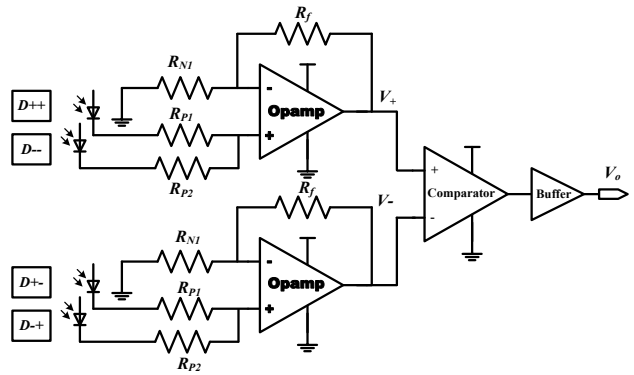


Fig 6. Detector Arrays and Comparators

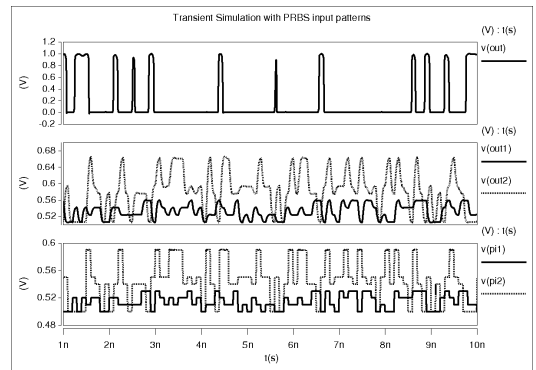


Fig 7. Optical Receiver Simulation Results

3. Design Considerations of VCSEL Arrays and Photodetector Arrays

A. Timing Synchronization of VCSEL Arrays

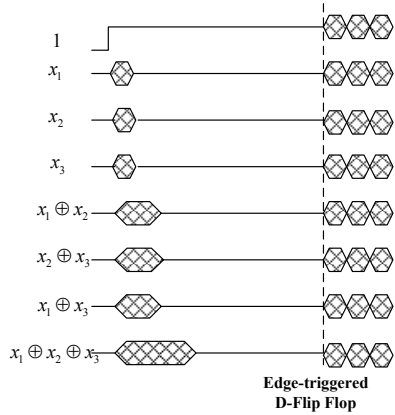


Fig. 8 Time Synchronization of VCSEL Arrays

From Fig. 5, we show a circuit to implement a three variables truth table mapping, therefore, we understand that different circuits to implement the Boolean basic vectors has different time delays as shown in Fig. 8. Signals have to go through different signal paths. We need a synchronization mechanism to turn on/off the VCSEL arrays at the same time. Such time synchronization can make sure that the correct switching times of truth-table outputs in the optoelectronic system.

B. Two Different Methods for the Optoelectronic System Design

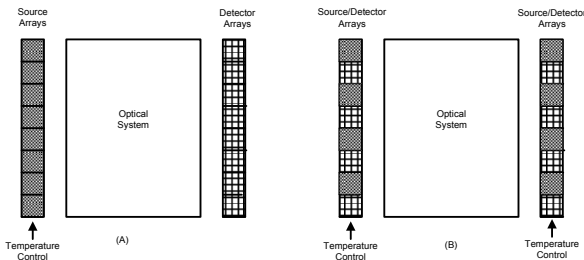


Fig. 9. Two different methods for the optoelectronic system design in optical interconnects (A) Source Detector arrays in the different planes (B) Source Detector arrays in the same plane

There are two different methods for optoelectronics system design in optical interconnects. The first method is to separate the sources and detectors in two different planes [15-16]. The second method is to integrate sources and detectors in the same plane [19-20], this is illustrated in Fig. 9. The major advantage of the first method can reduce the alignment error of the optoelectronic system. Since VCSELs and detectors are two types of different material [19-20], it is easier to design temperature control circuits for two types of material in two separated planes. If we integrate the sources and detectors in the same plane, this may cause extreme difficulty in designing temperature control circuits. In addition, the second method will have serious issues on alignment errors [17][18].

C. Temperature Issues In Optoelectronic Interconnect System Design

To the best of our knowledge, John .A. Neff was the first to suggest thermal considerations of free space optical interconnects using VCSEL based smart pixels and made significant contributions [21]. In free space optical interconnects, since the high temperature rising become an critical issue, there is less problem if we are only considering one or two VCSELs, however, for a large array of 256 x 256 matrix type of VCSELs, this will consumed large power.

In Figure 10, we show a 8 x 8 VCSEL arrays. Figure 11 shows an actual implementation diagram of VCSEL arrays in AIN substrate [23]. One of the key undesirable functions of VCSEL is the compilation of heat inside the laser cavity. Self generating high heat of VCSEL can accumulate excessive heat source, which limit the performance of VCSEL arrays, mainly due to it's internal high current density build up in the doped Bragg reflectors (DBRS). The increasing in temperature causes the increase the threshold current density, plus reduce the output power, and shift frequency to longer wavelength, in addition, it may reduce its lifetime. D. Botez [24] and S.Fu [25] indicate the steady state thermal rate equation inside cavity of VCSELs as following:

$$\rho_m C_p \frac{\partial T}{\partial t} = \nabla \cdot (k_r \Delta T) + \rho_T \dots \dots \dots (3)$$

Where ρ_m is the mass density, C_p is the heat capacity, k_r is the thermal conductivity of the laser cavity, ρ_T is the power density. D. Botez [24], S.Fu [25] and N.Bertra [26] did an excellent work on single VCSEL thermal analysis. They tried to extend the work through arrays of VCSEL using finite difference method and finite element method, however, the heat distribution on VCSELs array was difficult to estimate through those numerical methods.

We are curently working temperature estimation of evenly distributed two dimensional VCSELs array and temperature control circuits.

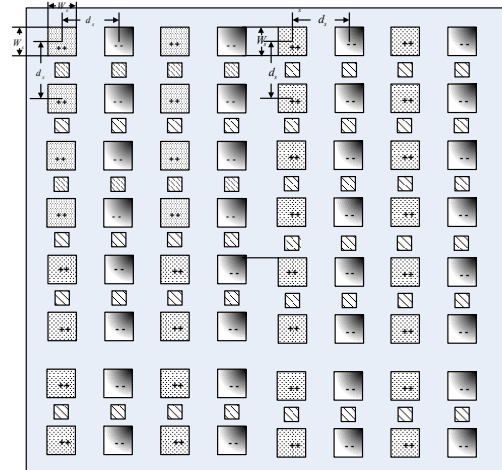


Figure 10. A 8 x 8 VCSELs array temperature estimation [4]

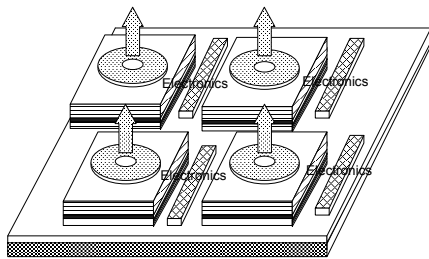


Figure 11 VCSEL arrays in AlN substrate [23]

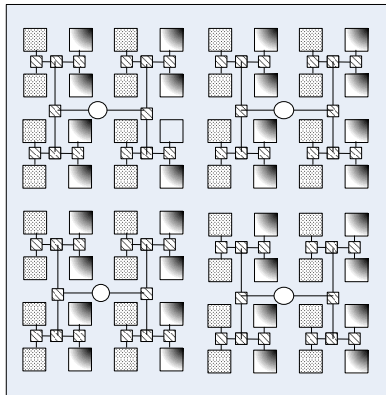


Figure 12. A 8 x 8 VCSELs array based on UCSD's work [5]

4. Conclusions and Acknowledgement

In previous works [5-6], authors did not show the detail calculations on how to implement the digital interconnect in optoelectronic interconnect networks. We showed [4][7] the calculations and methods to implement the Banyan switching network in optoelectronic implementations.

We also provide a solution to synchronize the VCSEL source arrays in time domain.

Temperature control becomes a critical issue of large VCSEL source arrays, the previous methods can not provide such calculations. We are currently working on a possible solution to this problems.

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