The Realization of Gray Scale Control for AM-OLED Based on Fractal theory^{*}

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Abstract - Fractal theory was firstly applied in gray scale control of Active Matrix/Organic Light Emitting Diode (AM-OLED) display system, which settled the problem of time redundancy of traditional scanning methods. In the experiment, a fractal scanning controller was designed and applied in a AM-OLED matrix display with 12 by 12 pixels. Timing simulation results indicate that compared with the traditional scanning methods, the novel method can improve scanning efficiency evidently, especially in the case of high gray scale and large screen. Therefore, the method provides a new way to solve the bottle problem of high articulation multimedia FPDs development.

Index Terms - Gray scale; time redundancy; fractal theory; AM-OLED.

1. Introduction

With the rapid development of information technology, the requirement of information and display technique for people grows higher and higher. So FPD (Flat Panel Display) with rich color 、 low cost 、 green 、 lightweight 、 and even flexibility, has become a goal of modern people to seek. OLEDs would be an ideal technology for information display due to its low driving voltage, highly efficient luminescence, rich color, fast response, wide viewing angle, portability, and etc [1-3].

OLED is a device of current-driving. Because of the difference in manufacturing process of pixels or driving transistors in AM-OLED [4, 5], it is difficult to achieve the consistency of all pixels having the same voltage - current characteristic. So OLED display should have a set of driving circuits suitable for itself. At present, the realization of high gray scale generally using conventional time-modulation method [6, 7], which can eliminate the impact of the inconsistency of electrical characteristic for each pixels, but that still do not meet the requirements of high definition for AM-OLED display. With the increasing of AM-OLED panel size and gray-level, the scan-drive time for each frame image and the delay of data transfer are both shortened, which leads to the image flicker [8-10]. In order to reduce the speed of data transfer, such as dividing the display into small cells, and orderly scanning the display pixels of each cells by row, column and frame to obtain the gray scale display, which will inevitably increase the production cost of the driving circuits for the flat panel display. Therefore, the time waste produced in the scanning process results in the bottle problem of high articulation multimedia FPD's development.

XU Mei-hua etal [11] studied the optimal scanning scheme of gray scale imaging based on the fractal theory, proposed the optimal scanning architecture and its fractal model for FPD. The theoretic model and its fractal control strategy solve the bottle problem of transfer speed from memory space to display plane, and eliminate the time redundancy produced in FPD's gray scale imaging process. This paper based on the theoretic model designed a Fractal Scanning Controller, which was applied in a AM-OLED matrix display with 12 by 12 pixels. The experimental results indicate that the fractal scanning controller can improve scanning efficiency and image quality without changing the scanning frequency of flat panel display system, and eliminate the time redundancy produced in the FPD's gray scale imaging process by conventional methods.

2. Traditional gray scanning method

Traditionally, gray scanning driving include space and amplitude approach, while for the high definition FPD, digital gray methods are adopted, including time-division $\$ pulse width modulation (PWM) frame rate control(FRC) $\$ or sub-field algorithm. Among all the methods, PWM [12] including direct gray and bit weights scanning is currently the most common methods in the FPD.

A. Direct gray scanning

Direct gray scale scanning comparing the gray value with the timer value continuous outputs the logic effective value. The eight gray scale scanning sequence is given in Table 1. As can be seen from Table 1, the gray scale is 2^n (n represents bit width), and the scanning cycle is divided into 2^{n-1} time slice.

Gray Scale	Scanning No.									
	1	2	3	4	5	6	7			
0	0	0	0	0	0	0	0			
1	1	0	0	0	0	0	0			
2	1	1	0	0	0	0	0			
3	1	1	1	0	0	0	0			
4	1	1	1	1	0	0	0			
5	1	1	1	1	1	0	0			
6	1	1	1	1	1	1	0			
7	1	1	1	1	1	1	1			

Table 1. Direct gray scale scanning sequence for 8-levels gray

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The gray scale of direct gray scanning is proportional to the number of scanning times, and as the gray levels increasing, the number of time slices becomes larger. Finally unit time slice will be more than the unit delay of data transfer, which will not be able to complete data transfer and scan the full screen. Thus, the traditional direct scanning method is not suitable for high-resolution and high-definition FPD products.

B. Bit weights gray modulation

Bit weights gray modulation controls the scanning driver to output logic effective value according to the weights of the gray [13]. Suppose each pixel in the image using n data bits to represent its gray value ($N=2^n$ gray levels), any one pixel of the image, in order to achieve its desired display gray scale, the data of lowest bit of the pixel is firstly sent to the display system and delayed a fixed time which defined by the lowest bit according to the corresponding weight value. Accordance with the order, until the data transfer of the highest bit is completed, the gray effect of the pixel is demonstrated. The bit power scanning sequence of 8 grey scale is shown in Table 2, "R" represents logic effective scanning , and the subscript of the "R" represents data bit, "*" represents ineffective scanning.

Table 2. Bit weights scanning sequence for 8-levels gray

	SCANNING NO.									
GRAY SCALE	1	2	3	4	5	6	7			
	R ₀	R ₁	*	R_2	*	*	*			
0	0	0	0	0	0	0	0			
1	1	0	0	0	0	0	0			
2	0	1	1	0	0	0	0			
3	1	1	1	0	0	0	0			
4	0	0	0	1	1	1	1			
5	1	0	0	1	1	1	1			
6	0	1	1	1	1	1	0			
7	1	1	1	1	1	1	1			

Comparing Table 1 with Table 2, it is found that with the gray scale increasing the method of bit weights gray scale scanning is superior to the method of direct gray scale scanning. But with the gray levels increase, the refresh frequency of the display panel for both methods will rapidly increase, which leads to a contradiction between gray scale and frame frequency. At the same time, the time waste produced in the scanning process of bit weights scanning results in the bottle problem of high articulation multimedia FPDs development. For example, in Table 2, the effective scanning is respectively $R_0 \ R_1 \ R_2$, the scanning number is respectively $1 \ 2 \ 4$, the empty wait operation is four times, and the scanning number is respectively $3 \ 5 \ 6 \ 7$. So scanning efficiency= effective scanning times / total scanning

times=3/7=43%. The empty wait operation is referred to as time redundancy. Therefore, to improve the scanning efficiency, it must eliminate time redundancy.

3. Fractal Theory

A. Optimal scan structure

A image with 2^b (b represents bit width) gray scale, according to the linear or non-linear bit scanning method, in which each pixel is scanned b times, and the time intervals among b times scanning at least are respectively 2^{b-1} , 2^{b-1} $^2 \cdots , 2 \cdot 1$ (the last time interval 1 is the interval between the last point in the current cycle and the first point in the next cycle). In order to scan other points during the period of the two adjacent scanning waiting for the same point, the display space is divided into $Mn=2^{b-1}$ sub-space, each of which has b scanning points. So the number of total scanning points is b2^{b-} ¹. Moreover, these points must be scanned at different time, and any time only a point must be scanned. So the time depth of scanning is b2^{b-1}. It can be concluded that the necessary condition of the highest scanning efficiency for a scan structure is that the space is divided into 2^{b-1} and the time depth of scanning is b2^{b-1}.

With the number of bits increasing, the scanning diagram gradually tend to be an infinitely divisible self-similar fractal, which is equivalent to an ideal case of optimal scan structure of high bit within limited time and limited space. Figure 1 is the fractal structure of b equal to 16, Figure 2 is the fractal structure of b tending to infinity [11].



Figure 1. The fractal structure of b equal to 16



Figure 2. The fractal structure of b tending to infinity

B. Optimal scan structure

The structure of fractal scanning controller is shown in Figure 3, and each of the parameter is defined as follows:

NB is the bit width of Bit code, depending on the gray scale; NS is the bit width of sub-space code, depending on the scanning method. An image with n bits gray, the gray scale is 2^n . According to the fractal scanning algorithm, the number of sub-space divided is 2^{n-1} , and the bit width of the sub-space code NS is equal to (n-1). Moreover, the function of the controller is to complete the logic realization of fractal scanning algorithm. At the rising edge of the clock CLK, and with the signal GetNext logic effective high the controller outputs the sub-space code Segment [NS-1], bit code Bit [NB-1], and blanking code Hidden at the current time, to control the address of rows and columns and gray value.



Figure 3. The logical structure of fractal scanning controller

In this paper, the sub-space code Segment [NS-1] is used as row select signal, and the bit code Bit [NB-1] is used to determine the scanning time of corresponding row selected. For example, the 256-level gray simulation waveform of the controller is shown in figure 4, in which the frequency of clk is 10MHz, the width of bit code NB is 3. As can be seen from figure 4, when the controller scans the 32 sub-space (Segment equal to 32), the corresponding data bit is 7; when the next rising edge of the clk comes, the controller will jump to the 96 sub-space (Segment equal to 96) to scan, and the corresponding data bit to be scanned is 6.



Figure 4. 256-level gray simulation waveform

4. Application

A display system is shown in Figure 5, including a Display composed of 12 by12 AM-OLEDs, Row and Column

driver circuit, Data processing module, and Fractal scanning controller.

The structure of Data processing module is shown in Figure 6. As can be seen from the Figure 6, the Data processing module consists of register group, which is used to store one frame datas to be displayed. In order to improve the efficiency of data transmission, the register group is equally divided into two sub-groups. So, when one sub-group is used to store the next frame datas, another sub-group is used to output the current frame datas. Then, the Segment (sub-space code) signal determines which sub-space need to be scanned, and finally the Data_disp signal outputs the datas to the Display. The timing diagram of Data processing module in one frame time is shown in Figure 7.

If the refresh frequency of the Display is 100Hz, and the gray scale is 256. According to the traditional pulse-width modulation method, the dot clk frequency of the Display system is 3.69MHz, while by using Fractal scanning controller, the dot clk frequency of the Display system is 129.6KHz. So, by compared, it can be concluded that fractal algorithm can effectively reduce the scanning frequency of the system, especially in the case of large screen and high gray scale. The timing diagram of display system is shown in Figure 8.



Figure 5. The structure map of Display system



Figure 6. The structure map of Data processing module



Figure 7. Timing diagram of Data processing module



Figure 8. The timing diagram of display system

5. Conclusion

Fractal scanning controller was designed on the basis of the fractal theory, and applied to the gray scale scanning control of the AM-OLED display system. Through simulation experiment it is proved that the method can improve scanning efficiency and image quality without changing the scanning frequency of FPD system, and eliminate the time redundancy of FPD gray scale imaging process by conventional methods. Therefore, the fractal scanning algorithm provides a new way to solve the bottle problem of high articulation multimedia FPDs development, having high practical and economic value.

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