Reform and Practice of "Intergrated Circuit (IC) Layout Design" Course in the Vocational College

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Abstract—**IC layout design is an important course of micro electronic specialty in vocational college. But for the reason of teachers' lack of real working experience in enterprises, the course is disjointed from enterprises. By co-work with the IC design company and the help of the engineers, a reform of the course was done. By using modern EDA tools and through new teaching methods, the practice of the course was done in SZPT, and we got a reasonably good result.**

Keywords-EDA; IC;layout;course reform; vocational

I. INTRODUCTION

IC layout design means the lithography mask layout design, which is an important course in micro electronic technique specialty in vocational college and regular college [1-3]. The purpose of the course is to teach the ways and the tools to design the layout of Integrated Circuit (IC). IC design is a major occupational direction in micro electronic field [4, 5]. Among this IC design industry, "IC layout design "is rather a good post for vocational college students. To most vocational college in China, the teachers in the college do not have the experience in a real IC layout design work, so the original course plan is separated from the industry area, the content is outdate and the teaching methods are not so effective to train the students how to work. For this reason, the course reform is very urgent and essential.

II. ENTERPRISES PROJECT BASED COURSE TEACHING CONTENT

A. The Choice of Real Projects form Enterprises

The teaching content is one of the most important parts of a course. In this paper we chose a SRAM project which is a real project in an IC design enterprise as the training project for the class. To chose SRAM has some advantages. As we know, SRAM is a storage circuit which contents several components including: storage cell, sense amplifier, column decoder and row decoder. Among these components storage cell is design as a kind of array, column decoder and row decoder are digital circuit and sense amplifier is a typical analog circuit. So the project includes all kinds of circuit to be studied.

At the same time SRAM is a classic circuit which is contained by almost all kinds of large scale IC. It is the most common layout done by a layout engineer, and the design ways and principle of SRAM circuit is quit mature .To be teaching materials, the scale of SRAM can be modified easily to fit the students with different background levels

B. Analysis of The Teaching Materials

The SRAM circuit contains four parts, and each part has its own working principles. The storage cell is a six-MOSFET stander circuit, and the key points to design the module are to make the area of the layout small and how to make a better floor plan. The sense amplifier is a kind of differential amplifier, which contains several NMOS and PMOS transistors. The key point of sense amplifier is how to design symmetrical transistors. The column decoder and row decoder are digital logic circuit which are composed of DFF, transmission gate, AND gate, NAND gate, OR gate, NOR gate, XOR gate and so on. The key point is to understand the working principle and design ways of these kinds of logic gate.

By analyzing the SRAM, we can draw a conclusion that each module of the project contains some same small cells, which is shown in Fig. 1.
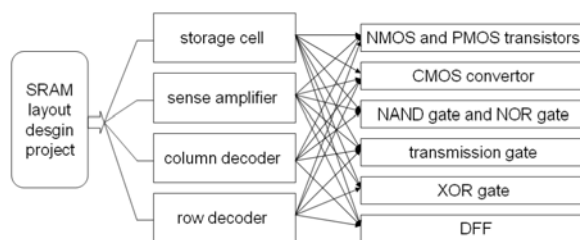

Figure 1.   Fig.1 components of each part in SRAM

Each module contains NMOS/PMOS transistors, which is the basic comment of any modern IC. So, how to achieve NMOS/PMOS layout design is very important to this course. Most parts of the SRAM contain stander logic circuit, so CMOS convertor, NAND gate and NOR gate were chosen as course content.

The transmission gate and XOR are not only stander logic circuit but also useful component of the circuit. The transmission gate is also used in the storage cell of SRAM and the XOR are good example to practice symmetrical transistors design. The transmission gate and XOR were also chosen as course content.

The DFF is so important that almost none circuit can work without it. Although it is a littler difficult than the other units of learning, it is the necessary part of this class.

C. Organization of the Teaching Content

As see above, there are four modules to construct the SRAM project, so the six modules are the basic content to be studied in this course. But the six modules are not at the same logic level meanwhile. As we know, the COMS convertor, Logic gate and any other circuit are composed of N/PMOS, so the first step is to learn how to design the layout of it. We compare layout design of the N/PMOS as the bricks, and set it as learning situation 1. The relationship of the modules was shown in Fig.2.
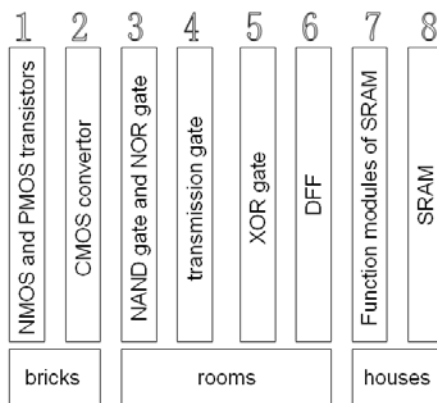

Figure 2. The relationship of the learning situations

The CMOS convertor, the NAND/NOR gate, the transmission gate, XOR gate and DFF are composed of N/PMOS, so they are compared as the rooms which are composed of bricks. The five modules above are set as learning situation 2 to learning situation 6. After the six learning situations, the four pars of the SRAM will be taught. The teacher will divide the students into several groups, and each group will design the four parts with internal division of the job. Finally, each group will finish just one SRAM design by co-work. The SRAM and the four parts of the SRAM are very similar to the houses or tall building which is composed of rooms.

III. TEACHING METHODS AND TEACHING MEANS

A. The Usage of EDA Tools Synchronizing with Industry

In most high school, the IC layout design course is done by some old EDA tools or even by coordinate paper. The old EDA tools such as "Tanner EDA" is scarcely used in the industry filed. So the student will not easily adapt to the work.

Nowadays, most IC design company (fabless) use "Cadence IC Design Frame work" as the basic layout design tool. To use EDA tools synchronizing with industry, SZPT (Shenzhen Polytechnic School) bought the EDA tool form Cadence Company, and uses the stander PDK (Process Design Kits) from Chinese domestic IC foundry.

Beside "Cadence IC Design Frame work", the Aether EDA tool, which is a production of Huada Empyrean Software Company, is also a popular layout design tool. By co work with Empyrean, the teachers in SZPT had finished the Aether EDA tool course in Empyrean, and the Empyrean provided some PDK and run set files for the class.

B. Co-work with Enterprises to Get Better Teaching Efficiency

In the renewing of the course, the key point is the lack of practical experience. Most high school teachers don't have the opportunity to design any layout in a real project, so they don't know the ways how to design layout exactly. By co-work with IC design enterprises can handle this problem. The ways of cooperation was shown in Fig.3.
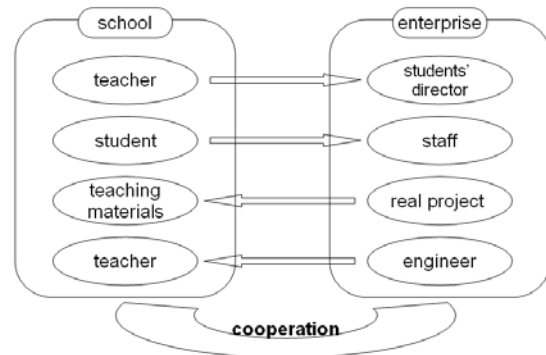

Figure 3. Cooperation between school and enterprises

Firstly, the engineers were invited to school as the instructor, and the teachers from high school worked as assistants. When the engineers came to school, they took the real project along with themselves. Also, some students have the opportunity to join the work team in the enterprises, which are chosen by the engineers form enterprises.

The teachers also need to go out with the students, and to be the directors of the students in enterprises. With the help of the enterprises, we built up an environment witch is same as what the engineer is facing in company.

C. Make Full Use of Teaching Website

The IC layout design course in SZPT has already been the national quality course, and it has an impeccable website to help students learn more. The website has three major function, including "on line test", "on line games" "knowledge repository".

The "on line test" is a platform which can provide some sets of test papers for each learning situation. After test, the mark will show up automatically. On the website, we also provided some flash games which are related to the content in the course to provoke the students' interests. Finally, we set a great amount of materials on the website and we call it "knowledge repository". The "knowledge repository" contains the layout examples in the class, the working

experience from the layout engineers and the video records of the class.

IV. EVALUATION MODE ASSESSMENT METHODS

In most traditional class, there is a final exam to evaluate the students' learning, but there is not a final exam in this class. During the 8 learning situations, the students will take a formative assessment. For each learning situation, the students will be evaluated form five aspects as shown in Fig.4.
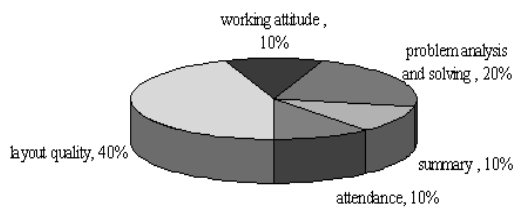

Figure 4. Five-aspect evaluation method

In each learning situation, the layout quality will take 40% of the score, working attitude will take 10% of the score, problem analysis and solving will take 20% of the score, summary will take 10% of the score and attendance will take up 10% of score. So the final score can be calculated by the following equation (1):

$$Final\ score = \sum_{N=1}^{8}(0.4A + 0.1B + 0.2C + 0.1D + 0.1E)/8 \tag{1}$$

In the equation, A means score of layout quality, B means score of working attitude, C means score of problem analysis and solving, D means score of summary and E means score attendance.

V. CONCLUSION

Through the course renew, there are some remarkable achievements were done in SZPT. First and foremost, the average period of getting familiar with the job became much smaller. Secondly, the students' interests on the course grew. Last but not least, the student can draw layout with Cadence tools or Empyrean tools much better than ever before. So, the course renew is good to students. At the meanwhile, the teacher got to know many layout skills in real projects from the enterprises, which is also good to the course.

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