Design and Implementation of FSK Modulation and Demodulation Module Using CPLD

Lihua Wu, Yu Huang

College of Science, Harbin Engineering University Harbin, Heilongjiang, China
wulihua@hrbeu.edu.cn, huangyu_cge@china.com.cn

Abstract - According to the working principle of digital FSK modulation and demodulation, two kinds of circuit schemes based on CPLD and single chip are compared. The circuit module of FSK modulation and demodulation based on CPLD is designed, and CPLD is programmed by Quartus II software to carry out the function of FSK modulation and demodulation. The single chip ATMEGA16 is programmed by IAR FOR AVR software to carry out the function of bit synchronization, and it can communicate with outside by SPI interface. Both simulations and experimental tests prove the exactness of design through building up the actual circuit.

Index Terms - FSK modulation and demodulation, CPLD, single chip, bit synchronization

I . Introduction

Digital modulation and demodulation is an important topic of modern communication. In the communication system, base-band digital signal includes abundant low-frequency signal. It is essential that the power spectrum is moved to higher carrier frequency via carrier modulation of digital signal in order to transfer digital signal far in finite band-width channel or fiber. FSK(frequency shift keying) is a prior information transfer manner for its advantages in noise resistance, transfer distance and bit error rate, and therefore it is widely applied in medium or low speed data transfer in fading channel[1-2]. In recent years, scholars and corporations did their endeavors in research and popularization of modulator and demodulator. There have been a mass of productions of Bluetooth communication equipment, medical embedded microelectronics device and portable consumer electronics[3-8]. FSK modulation and demodulation can be designed by single-chip or CPLD[1,3]. In the scheme of single-chip, the occupancy rate of resource is higher, for example, an interrupt will happen every other 1/300ms for ATMEGA16. Because the single-chip deals with interrupt at most time, it is easy to snatch interrupt to make the modulation and demodulation system instable. Generally, the port operation speed of single-chip is at most 1MHz, and its baud rate of FSK signal is unable to very high. However, the port operation speed of common CPLD reaches 120MHz, so the FSK modulation and demodulation using CPLD can be design upper baud rate with the advantage of parallel run of CPLD program and escape of contest in hardware resource. We select the design scheme of FSK modulation and demodulation based on CPLD.

II . System Design

The schematic chart of working principle for FSK signal produced by one piece of CPLD is shown in Fig.1. The system clock provided by 100MHz oscillator is used to be local oscillation, which become carrier waves with frequencies f1 and f2 via the first and second dividers, respectively. The two carrier waves are connected with a gating switch, who selects corresponding carrier wave according to logic input. The carrier wave with f1 will be selected when input is '1', and carrier wave with f2 will be selected when input is '0'. FSK signal will be produced through selection of carrier waves with different frequency.

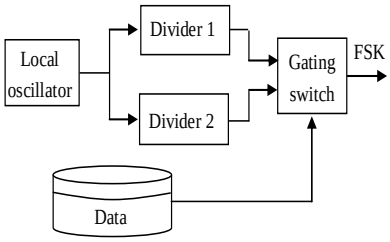

Fig. 1 FSK modulation principle based on CPLD

A zeros-crossing detection method is used for FSK demodulation based on CPLD, which is suitable for digital implementation due to some advantage with simple structure, easy to realize, insensitive to gain fluctuation. The frequency of FSK is determined by the number of it crossing zero voltage axes in unit time. Before transferring to CPLD, FSK is taken out its amplitude through signal processing of limiter and amplification from pre-circuit. The schematic chart for FSK demodulation based on CPLD is shown in Fig.2, where the divider module of CPLD is used to broaden impulse, counter and rectifier modules is used for edge detection. The judging base band signal can be achieved by LPF (low-pass filter) module and the demodulation of FSK comes true.

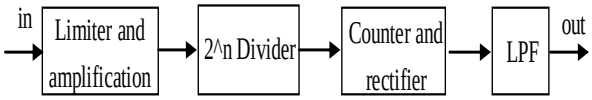

Fig. 2 FSK demodulation principle based on CPLD

The whole circuit chart of FSK modulation and demodulation based on CPLD is shown in Fig.3 with four modules including power, pre-signal processing, CPLD and single-chip control. A piece of MAX II series CPLD (EPM 240T100I5N) is used for modulation and demodulation,

and single-chip (ATMEGA16) is for a controller. The serial port is a digital communication system which includes asynchronous bit synchronization, so the demodulation signal can be directly reverted to digital signal by the serial port of

single-chip and then a SPI interface is set aside to communicate with outside via leaving out bit synchronization of CPLD .

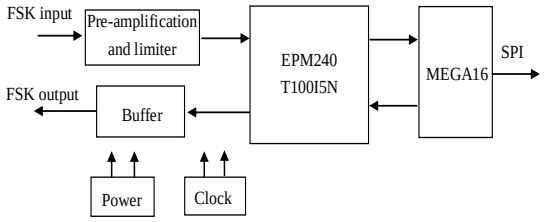

Fig.3 Circuit chart of FSK modulation and demodulation

In the procedure of modulation, single-chip transmits serial data including start bit, stop bit and a parity check bit to CPLD by serial port TXD. FSK can be produced via modulating the base-band signal from CPLD, and more is transmitted through a buffer. The procedure of demodulation is opposite to modulation. Firstly, FSK is introduced to CPLD after limiting and amplifying through pre-processing module. Secondly, FSK amplified is demodulated by CPLD and transmit to single-chip through TXD. Finally, the serial port carries out bit synchronization to pick up data, which is exported via SPI.

III . Design of System Software

The logical structure of FSK modulation module is designed by VHDL as shown in Fig.4, and the signal of interface is defined as followed. Clk: carrier wave of FSK modulation. It is shaped by 8 and 4 times frequency divider composed of an inner three-bit counter, which counts clock provided by 10MHz oscillator in the rising edge of it. Data: input port of data, namely input port of base-band signal. Fsk_out: output port of FSK modulation. When data is high, fsk_out is connected with four times divided frequency via select switch, and with eight times divided frequency when data is low. The modulation of FSK comes true.

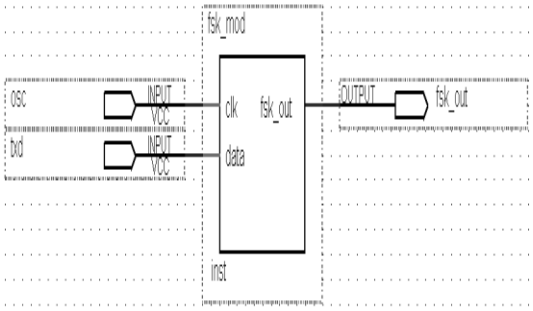

Fig.4 FSK modulation module

The logical structure of demodulation module is designed as shown in Fig.5. At the rise edge of the signal fsk_sig, the module de_fsk is triggered to save counter[7…0] to inner 8-bit register. Both they and synchronous signal are exported by tri_count. The module de_fsk2 is to assign tri_count to the two registers count1, count2 in the role of synchronization signal and to export flag_out, which is used to judge the time sequences of two registers. In the module de_fsk3, the signal flag_out make count1 minus count2, and the effect of counter reset is eliminated by algorithm to obtain the period of FSK. The output of de_fsk is ‘1’ or ‘0’ according to the period.

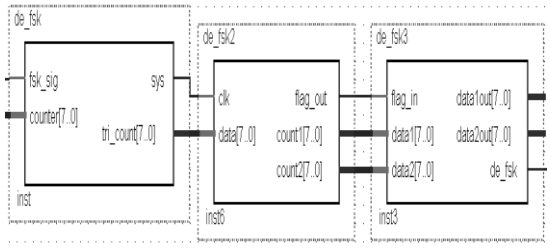

Fig.5 FSK demodulation module

IV . Experimental Test

The simulation based on Quartus II software is shown in Fig.6, where osd represents the input of clock with frequency 10MHz, txd is data input port, fsk_out is FSK modulation output. From Fig.7, we can know that the frequency of fsk_out is 2.5MHz when data is ‘1’ and 1.25MHz when data is ‘0’. It means that the module of modulation can work in order.

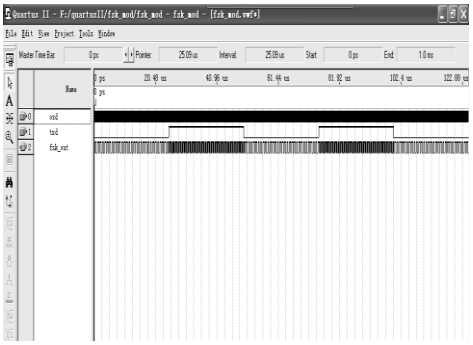

Fig.6 Simulation of FSK modulation module

Because the waveform simulation of Quartus II can’t directly add FSK signal, all pins add in waveform simulation program in order to attach modulation module output to FSK input port of demodulation module. In this case, the simulations are shown in Fig.8, where osc represents the input of clock with frequency 10MHz, txd is input port of FSK modulation module, de_fsk is FSK demodulation output. The modulation signal of modulation module is interiorly connected with input port of FSK demodulation module.

From Fig.7, we can know that the signal demodulated is the same with the corresponding input, and it means that the module of demodulation can work in order. However, race hazard will happen in the procedure of demodulation, so there are many flashes in the demodulated signal. It is necessary to design a filter module after demodulation to clear these flashes. The fabricated circuit of FSK modulation and demodulation is shown in Fig.8, which is composed of two pieces of circuit broads with CPLD. One is used for FSK modulation and other is for FSK demodulation. They are connected together by a triaxial cable.

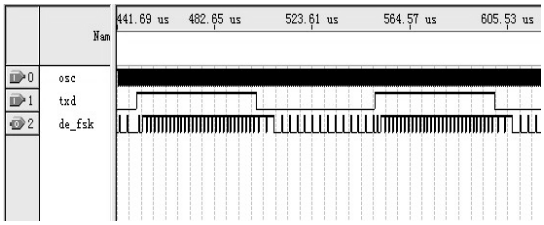

Fig.7 Simulation of FSK demodulation module

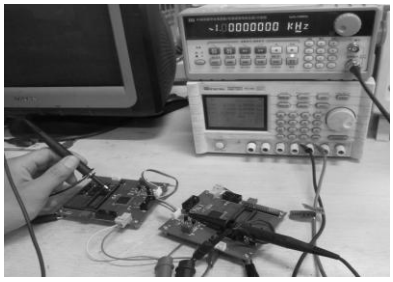

Fig.8 Fabricated circuit of FSK modulation and demodulation based on CPLD

A multi-function signal generator creates a square wave with the frequency of 10 kHz, the peak-to-peak amplitude of 3.3V, the DC bias of 1.65V, which is introduced into the base-band input port of CPLD. The test results about FSK modulation and demodulation are observed by oscilloscope as shown in Fig.9, where the waveform of the first channel is FSK modulation signal and that of the second channel is the signal via demodulation and filter based on CPLD. The RC-type filter with cut-off frequency of 40kHz can smooth the demodulation signal. The data via demodulation and filter is the same with the modulation signal. Experimental tests prove that the highest frequency of modulation signal based on CPLD can arrive at 15kHz. It means that its baud rate with 30kbit/s can come true, whose speed is determined by exchange rate between SPI port of single-chip and USART.

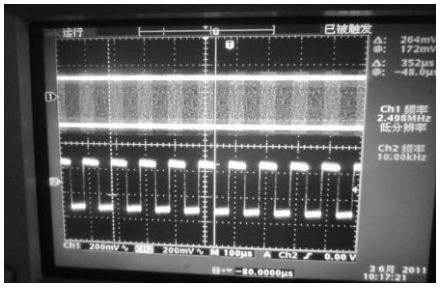

Fig.9 Experimental results of FSK modulation and demodulation

V . Conclusion

Two kinds of schemes of FSK modulation and demodulation based on single-chip and CPLD are compared and analyzed. The whole project FSK modulation and demodulation based on CPLD based on is put forward. A full-digital circuit of FSK modulation and demodulation based on MAXII serial CPLD is designed, and the program of each module is written and validated by simulation. The experimental tests on the circuit show that it can work in order with these advantages of simple structure, good reliability and strong capability of anti-jamming.

VI . Acknowledgment

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