- If the simulation is complex it obliges to oversize the execution platform to meet the real time constraints.

The solution implemented to overcome this problem was called “time virtualization”: a simulated clock is implemented between U-TEST system clock and operating system clock. In practice the mechanism can be compared to software Phase Locked Loop (PLL) controlled by the simulation execution Overrun Time Margin(OTM). OTM can be seen as time difference between model real execution time and model specified execution period. When OTM is important (for instance a 10 ms periodic model executes in 1 ms) the virtual clock frequency increases and vice-versa.

In practice simulation is started with very low simulated clock frequency to avoid initial overrun. Simulated clock speed is progressively adjusted (increased) to maximize simulation execution time.

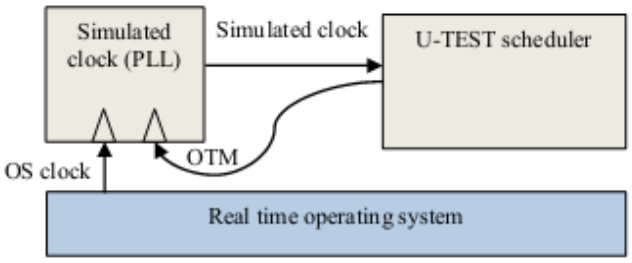

Fig. 9 Simulated clock principle

This mechanism is activated for pure virtual test mode only. If real hardware is in the loop OS real time clock is used.

IV . Conclusion

This paper presented a novel approach to extend a hard real time test platform to perform avionics virtual test.

Cassidian Test&Services demonstrates with U-TEST that both software and hardware technologies are ready to face the challenge of test system unification in the avionic IVV process.

The next steps to ensure a real take off of such technologies are:

- The emergence of standards: this new avionic test strategy needs standardization to ensure exchange of data, models and test cases between the players (System Manufacturers, Equipement Manufacturers, subcontractors)

- The convergence of test processes within the big companies (System and Equipment Manufacturers) with a common purpose:test activities have to be anticipated in early design phases.

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