

On the MAP-Level Delay Reduction of Turbo Decoding

Sun-Ting Lin¹, Shou-Sheu Lin², Chuan-Wen Chiang²

¹ Department of Electronic Engineering, National Kaohsiung Normal University, Yanchao, Kaohsiung 824, Taiwan

² Department of Computer and Communication Engineering, National Kaohsiung First University of Science and Technology, Nanzih, Kaohsiung 811, Taiwan
stl@nknknu.edu.tw

Abstract - A time-offset scheme for the shuffled turbo decoding is proposed. The decoding latency of the proposed scheme is shorter than the serial turbo decoding by offsetting the decoding timing of two component decoders. Meanwhile, its BER performance is better than the shuffled turbo decoding. We found that the effective extrinsic information is the key for the BER performance. Simulation results show that our scheme can flexibly balance the decoding latency and BER performance.

Index Terms - Turbo Decoding, Delay Reduction, MAP.

1. Introduction

Turbo code¹ is a capacity-approaching error correction code and its bit error rate (BER) performance is close to the theoretical Shannon bound. Turbo decoding exchanges the extrinsic information from one component decoder to the other and repeats the decoding process several times to achieve better decisions. Due to its superior performance and reasonable decoding complexity, it has been widely used in many communication systems, such as the 3G WCDMA, WiMAX and 4G LTE-A.

In spite of the efficiency of iterative turbo decoding, the decoding latency caused by serial iteratively decoding is a bottleneck of decoding throughput. Thus, other turbo decoding structures such as parallel decoding², shuffled decoding³, and its variants⁴ were proposed to shorten the decoding latency. In the parallel decoding, all component decoders operate simultaneously. After finishing an iteration of decoding, each component decoder delivers the extrinsic information to other decoder as the a-priori information at the next iteration. Due to the decoding quality of first iteration is usually not reliable and its effect will propagate to the upcoming iteration of decoding, the performance is much worse than the conventional serial turbo decoding.

To fully utilize the reliability of newest extrinsic information up to current decoding bit, the shuffled decoding scheme was proposed. In shuffled decoding, the decoding structure is the same as parallel decoding scheme but the extrinsic information is exchanged bit-by-bit immediately to each other decoder rather than block-by-block after generating the whole block of extrinsic information for next iteration. The decoding speed is faster than the conventional serial decoding, however, the BER performance is worse.

This paper is organized as follows. In section 2, the turbo decoding structures are briefly reviewed. In section 3, the proposed skewed turbo decoding scheme is described in detail. In section 4, simulation results are reported and compared. Finally, conclusions are drawn in section 5.

2. Decoding Structures Review

As shown in Figure 1, the conventional serial decoding is essentially a decoding loop, which consists of a first maximum a-posteriori (MAP) decoder MAP₁, an interleaver π , a second MAP decoder MAP₂, and a deinterleaver π^{-1} in series. In that, the main function of the MAP decoder is to calculate the extrinsic information and a-posteriori probability (APP) and is usually implemented by the BCJR algorithm⁵.

After received a noisy turbo codeword, the MAP₁ calculates the extrinsic information L_{e1} based on the systematic information L_{s1} , the first parity information L_{p1} , and the first a-priori information L_{a1} . Note that the time index k is ignored here for simplicity. Then the extrinsic information L_{e1} is interleaved as the a-priori information L_{a2} for the second MAP decoder. Similarly, the MAP₂ calculates the extrinsic information L_{e2} based on the interleaved systematic information L_{s2} , the second parity information L_{p1} , and the second a-priori information L_{a2} . The second extrinsic information L_{e2} is deinterleaved to form the a-priori information L_{a1} for the MAP₁ decoder. One iteration is defined as running each element in the decoding loop once.

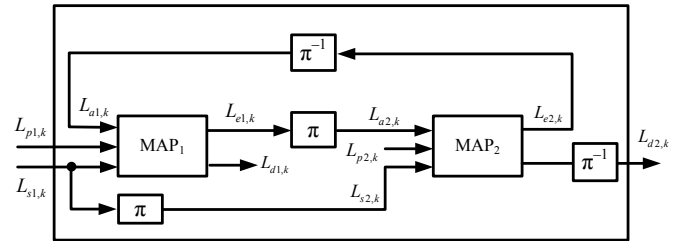


Fig. 1. Functional block diagram of the conventional serial turbo decoder.

To reduce the complexity, the MAP decoder is typically implemented by the logarithmic BCJR algorithm named as the Log-MAP⁶ algorithm. For convenience, the algorithm is summarized as follows. Note that the Log-MAP algorithm is the same for both component decoders, thus, we ignore the subscript notation for i th decoder for simplicity.

$$g_k(s', s) = \frac{1}{2} u_k(L_{a,k} + L_{s,k}) + \frac{1}{2} L_{p,k} x_k^p, \quad (1)$$

$$d_k(s) = \max_{s' \in S_{k-1}} \{g_{k-1}(s') + g_{k-1}(s', s)\} - H_k, \quad (2)$$

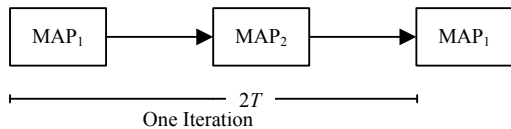
$$b_k^o(s') = \max_{s \in S_{k+1}} \{g_{k+1}^o(s) + g_k(s', s)\} - G_k, \quad (3)$$

$$L_{d,k} = \max_{(s',s) \in E^+} \{ \partial_{\hat{q}}(s') + \mathcal{G}_{\hat{q}}(s',s) + \mathcal{B}_{(k+1)}^{\hat{q}}(s) \} - \max_{(s',s) \in E^-} \{ \partial_{\hat{q}}(s') + \mathcal{G}_{\hat{q}}(s',s) + \mathcal{B}_{(k+1)}^{\hat{q}}(s) \}, \quad (4)$$

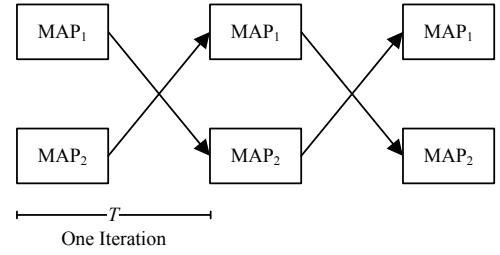
$$L_{e,k} = L_{d,k} - L_{s,k} - L_{a,k}, \quad (5)$$

where the subscript k is the k th time instant, $\mathcal{G}_{\hat{q}}(s',s)$ is the branch metric from a starting state s' to an ending state s , $u_k \in \{ -1, +1 \}$ is the value of the transmitted symbol, S_k is the set of total state at the k th time instant, E^+ / E^- is the set of (s',s) branch pair corresponding to $u_k = +1 / u_k = -1$, respectively; $\partial_{\hat{q}}(s)$ is the forward state metric, $\mathcal{B}_{\hat{q}}^{\hat{q}}(s')$ is the backward state metric, $L_{d,k} / L_{a,k} / L_{e,k}$ is the APP/a-priori information/extrinsic information, respectively; L_c is the channel reliability, y_k^s is the value of the received systematic information symbol, $L_{s,k} = L_c y_k^s$ is the log-likelihood ratio of y_k^s , y_k^p is the value of the received parity symbol, $L_{p,k} = L_c y_k^p$ is the log-likelihood ratio of y_k^p , x_k^p is the value of the transmitted parity symbol, H_k and G_k are the normalization terms for $\partial_{\hat{q}}(s)$ and $\mathcal{B}_{\hat{q}}^{\hat{q}}(s')$, respectively; and $\max^* \{a,b\} = \max(a,b) + \ln(1 + e^{-|a-b|})$.

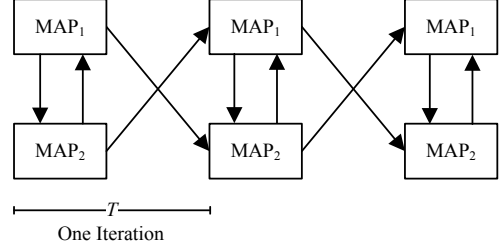
Different decoding structures of the previous works are described in Figure 2. For the conventional serial decoding shown in Figure 2(a), the extrinsic information of a codeword is delivered to MAP decoder sequentially. Each component decoder has to wait an entire block of delay for starting next MAP decoding. Let T be the decoding latency for completing a MAP decoding. The serial decoding spends $2T$ to finish one iteration. In contrast, the parallel decoding shown in Figure 2(b) performs both MAP decoders concurrently and then exchanges extrinsic information in next iteration. The parallel decoding spends T to finish one iteration. To improve the performance, the shuffled decoding shown in Figure 2(c) exchanges the extrinsic information immediately on the bit-by-bit basis. The shuffled decoding spends T to finish one iteration. Due to lack of fully utilization of the extrinsic information, both the parallel and shuffled decoding suffer from degradation of BER performance compared to the serial decoding.



(a)



(b)



(c)

Fig. 2. Turbo decoding structures of (a) the conventional serial decoding, (b) the parallel decoding, and (c) the shuffled decoding

3. Proposed Skewed Turbo Decoder

The idea of proposed scheme is to convince a method to improve the exchanging rate of the extrinsic information between two MAP decoders, meanwhile maintaining the BER performance. In this paragraph, the skewed turbo decoding is proposed and the analysis of the extrinsic information updated times and exchanging algorithm is derived.

A. Skewed Turbo Decoding

From section 2, we know that the advantage of serial decoding is good performance. The advantage of shuffled decoding is low delay latency. Leveraging on the advantages of the serial and shuffled decoding, the skewed decoding was proposed. As shown in Figure 3, an offset time Δ between MAP₁ and MAP₂ to start the decoding of the first bit is added at every iteration.

Due to such time offset, the proposed scheme can provide more effective extrinsic information than the shuffled turbo decoding. The effective extrinsic information is the extrinsic information with good reliable, which is obtained on the better a-priori information on previous iteration. Because the serial decoding is based on more effective extrinsic information than other decoding schemes so that its performance is the best. Only if more extrinsic information is exchanged but its value is unreliable, the performance will not be improved effectively. The parallel decoding suffers this problem so that its performance is the worst.

To obtain more effective extrinsic information, the MAP₁ decoder is turn off after completing its decoding. This is an important step otherwise the performance will be the same as the parallel decoding. From the viewpoint of MAP₂, extra extrinsic information during an offset time window is provided and the probability of obtaining more reliable extrinsic

information is increased. Finally, a better BER performance can be achieved.

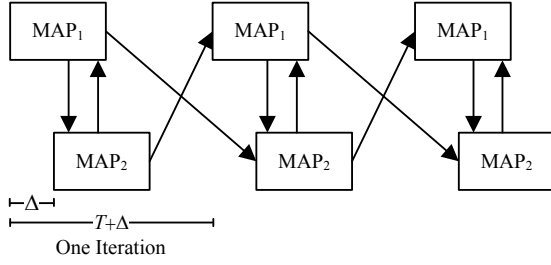


Fig. 3. Proposed skewed turbo decoding scheme.

B. Extrinsic Information Exchanging Algorithms for Skewed Turbo Decoding

In the shuffled decoding, due to the interleaver and deinterleaver is located between the two MAP decoders, the algorithm to calculate the reliable extrinsic information is dependent on the interleaving /deinterleaving pattern of and respectively. Define the interleaved bit location as (j) and deinterleaved bit location as (j) for j th bit. To deliver extrinsic information from MAP₁ to MAP₂ for the current iteration, the condition of $(j) < j$ must be satisfied, which means the extrinsic information L_{e1} of MAP₁ has to be generated and is ready for passing to MAP₂. On the other hand, the condition of $(j) < j$ should be fulfilled so as MAP₁ can obtain the extrinsic information from MAP₂.

Similar to the shuffled decoding, the extrinsic information exchanging algorithms of the proposed scheme to determine the a-priori information for MAP₂ is summarized as

```

for j = 1 to N
  if  $[\pi^{-1}(j) < \min(j + d, N + 1)]$  then
     $L_{a2}^i(j) = L_{e1}^i(\pi(j))$ 
  else
     $L_{a2}^i(j) = L_{e1}^{i-1}(\pi(j))$ 
  end if
end for

```

where N is the block length, d is time-offset in terms of bit, and its range is from 0 to N , $L_{a2}^i(j)$ is the a-priori information for the j th bit of MAP₂ at i th iteration, $L_{e1}^i(\pi(j))$ is the extrinsic information for the $\pi(j)$ -th bit of MAP₁ at i th iteration. If the condition $[\pi^{-1}(j) < \min(j + d, N + 1)]$ is true, the a-priori information $L_{a2}^i(j)$ is obtained from extrinsic information $L_{e1}^i(\pi(j))$ which is calculated from current iteration of MAP₁; otherwise, it is obtained from extrinsic information $L_{e1}^{i-1}(\pi(j))$ which is calculated from previous iteration of MAP₁.

Similarly, the algorithm to determine the a-priori information for MAP₁ is

```

for k = 1 to N
  if  $[\pi(k) < \min(k + N - d, N)]$  then
     $L_{a1}^i(k) = L_{e2}^i(\pi(k))$ 
  else
     $L_{a1}^i(k) = L_{e2}^{i-1}(\pi(k))$ 
  end if
end for

```

where $L_{a1}^i(k)$ is the a-priori information for the k th bit of MAP₁ and $k = (j + d)$, $L_{e2}^i(\pi(k))$ is the extrinsic information for the $\pi(k)$ -th bit of MAP₂ at i th iteration. For MAP₂, the larger the time-offset d will introduce higher probability of effective extrinsic information. In spite of reducing the effective extrinsic information for the first iteration of MAP₁, the overall exchanging rate of extrinsic information is increased.

In general, the proposed skewed decoding scheme can be applied to many existing MAP decoding algorithms. However, modification is needed to embed the skewed decoding scheme. Two type of MAP decoder were considered later for demonstration.

C. Exchanging Rate Analysis

If the exchanged extrinsic information is effective, the higher the exchanging rate the better the BER performance of the decoding system will be. Therefore, effective extrinsic information is the key for the BER performance. When updating the extrinsic information, the new extrinsic information is effective and the old extrinsic information is not effective. For shuffled turbo decoding scheme, MAP₁ and MAP₂ exchange extrinsic information bit by bit, therefore, some bits will use the new extrinsic information and others are not. Whether it uses the new or old extrinsic information depends on the interleaver function, \square and deinterleaver function, \square^{-1} .

The exchanging rate of the extrinsic information for MAP₁ and MAP₂ of different decoding structures can be described as the function of the k th iteration. Two functions, $f_{MAP1}(k)$ and $f_{MAP2}(k)$, are defined to represent the related exchanging rate of the first and the second MAP decoder for various decoding schemes.

$$f_{MAP1}(k) = \begin{cases} 2(k-1) & \text{serial} \\ k-1 & \text{parallel} \\ 1.5(k-1) + x & \text{shuffled, } k = \text{odd} \\ 1.5(k-1) + 0.5 & \text{shuffled, } k = \text{even} \end{cases}, \quad (6)$$

$$f_{MAP2}(k) = \begin{cases} (2k-1) & \text{serial} \\ k-1 & \text{parallel} \\ 1.5(k-1) + x & \text{shuffled, } k = \text{odd} \\ 1.5(k-1) + 0.5 & \text{shuffled, } k = \text{even} \end{cases}, \quad (7)$$

where x is the probability for $\square \square \square < j$. At the k th iteration, the final extrinsic information for MAP₁ has been updated $2(k-1)$ times in serial decoding but only $k-1$ times in parallel decoding. Similarly, the final extrinsic information for MAP₂ has been updated $2k-1$ times in serial decoding but only $k-1$ times in parallel decoding. The final extrinsic information exchanging rate of the shuffled decoding for MAP₂ at the k th iteration is approached to $(1.5k-1)$. Thus, its BER performance is between the parallel and serial decoding.

The exchanging rate of the proposed skewed turbo decoding scheme can be derived from equation (6) and (7) and summarized as below.

$$f_{MAP1}(k) = 2(k-1)\frac{D}{T} + 1.5(k-1)(1 - \frac{D}{T}), \quad (8)$$

$$f_{MAP2}(k) = (2k-1)\frac{D}{T} + 1.5(k-1)(1 - \frac{D}{T}), \quad (9)$$

where T is the decoding latency of one iteration, Δ is the offset time.

D. V-type and X-type Skewed Decoding

To demonstrate the performance, the proposed skewed decoding scheme is applied to two types of MAP decoders⁷. The V-type skewed decoding scheme is shown in Figure 4(a), where N is the information block length and n is memory length of the component code. During the backward recursion of first V-type MAP decoder, the backward state metric $\beta_{1,k}^0$ and the branch metric $g_{p,k}^0$ are calculated and no extrinsic information is generated during this period. Then the forward recursion is performed and the extrinsic information $L_{e1,k}$ is generated. Similarly, MAP₂ is delayed Δ time to decode. Note that the operation of interleaver, deinterleaver and the exchange of $L_{a1,k}$ and $L_{a2,k}$ are on the bit-by-bit basis.

The X-type skewed decoding scheme is shown in Figure 4(b). The forward recursion and the backward recursion of first X-type MAP decoder are performed simultaneously. Before forward and backward recursion meet each other, the forward state metric $\beta_{1,k}$ and the corresponding branch metrics $g_{p,k}$ are calculated from the beginning; and the backward state metric $\beta_{1,k}^0$ and the corresponding branch metrics $g_{p,k}^0$ are calculated from the end of the codeword. During this period, no extrinsic information is generated. Then, both recursions continue and the extrinsic information $L_{e1,k}$ are generated. Similarly, MAP₂ is delayed Δ time to decode. Note that the operation of interleaver, deinterleaver and the exchange of $L_{a1,k}$ and $L_{a2,k}$ are on the bit-by-bit

basis. Since the forward and backward state metrics are calculated concurrently, the decoding latency of the X-type is only half of the V-type.

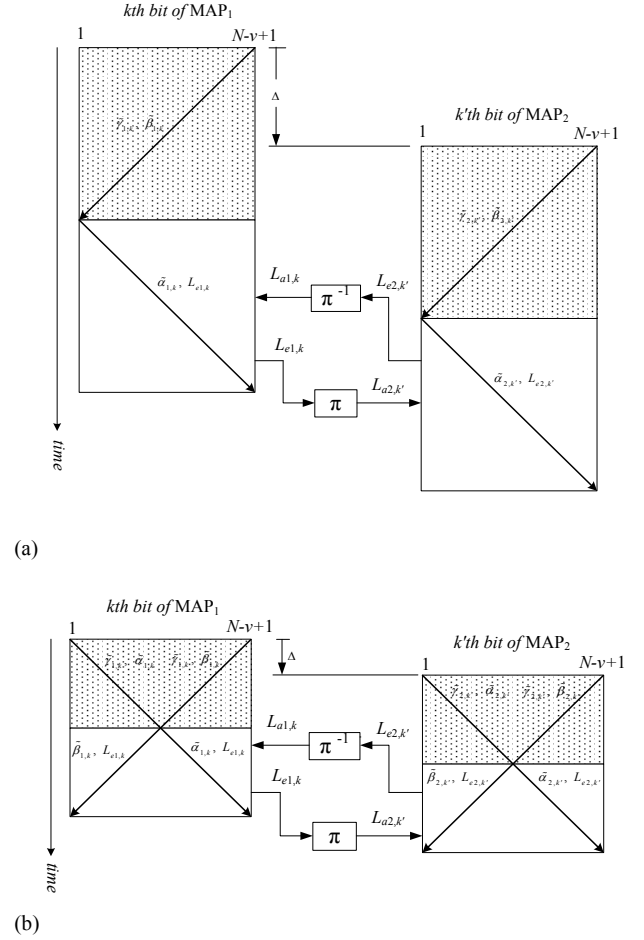


Fig. 4. Block diagram of the proposed skewed decoding with (a) V-type MAP decoder and (b) X-type MAP decoder.

4. Simulations

In order to demonstrate the efficiency of the proposed skewed decoding scheme, simulations were conducted to verify the performance. The simulation parameters are as follows. The turbo code constructed by parallel concatenating two (7,5) recursive systematic convolutional codes with zero-state trellis termination via a quadratic polynomial permutation (QPP)⁸ interleaver is used. The data block length is 6144 and the code rate is 1/3. The maximum number of iteration is limited to 8. The Log-MAP algorithm is used as the MAP decoding algorithm for each type of decoder. For investigate the effect of the offset time on BER performance, the offset time Δ is set to $1/4N$, $2/4N$, $3/4N$ and N , respectively.

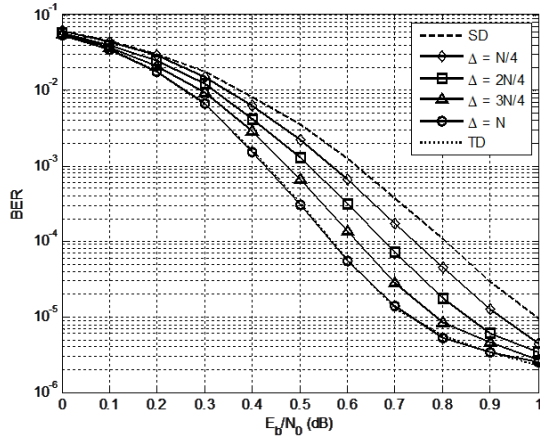
The BER performance of the proposed scheme for the V-type and X-type MAP decoders are shown in Figure 5(a) and Figure 5(b), respectively. As expected, the larger the offset time is, the better the BER performance is. For the V-type

MAP decoder, the BER curves are uniformly improved with the offset time. For the X-type MAP decoder, the BER curves are nonuniformly improved with the offset time. For small offset time, the BER performance of V-type is better than X-type. For large offset time, the BER performance of X-type is better than V-type.

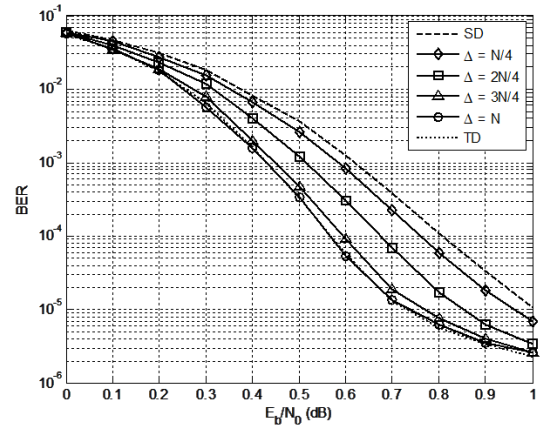
Ignoring the performance difference by using different type of MAP decoders, the BER performance of the proposed scheme with $3/4N$ offset time is close to the conventional serial decoding and the decoding latency is reduced effectively. When the offset time equals zero, the proposed scheme degenerates to the shuffled decoding (SD). When the offset time equals N , the proposed scheme degenerates to conventional serial turbo decoding (TD). Obviously, the performance of the proposed scheme is bounded between SD and TD and the proposed scheme can flexibly balance the decoding latency and BER performance.

5. Conclusions

A skewed turbo decoding scheme is proposed. The detail extrinsic information exchanging scheme and the exchanging rate analysis are provided. Simulation results for two types of MAP decoders are conducted to demonstrate the effectiveness. The proposed scheme provides a flexibility to adjust the BER performance and decoding latency between the conventional serial decoding and shuffled decoding. In general, many existing MAP decoding algorithms can be modified to accommodate the proposed scheme to reduce the decoding latency.



(a)



(b)

Fig. 5. Simulation results of the proposed skewed decoding with (a) V-type MAP decoder and (b) X-type MAP decoder.

References

- [1] C. Berrou, A. Glavieux, and P. Thitimajshima, Proceedings of the IEEE International Conference on Communications, (1993) May 23-26; Geneva, Switzerland
- [2] C. Argon and S. McLaughlin, IEEE Commu. Lett. 6, 70 (2002)
- [3] J. Zhang and M. Fossorier, IEEE Trans. Commun. 53, 209 (2005)
- [4] Y. Wang, J. Zhang, M. Fossorier, and J. S. Yedidia, Proceedings of the IEEE 6th Workshop on SPAWC, (2005) June 5-8; Hawaii, USA
- [5] L. Bahl, J. Cocke, F. Jelinek, and J. Raviv, IEEE Trans. Inf. Theory, IT-20, 284 (1974).
- [6] P. Robertson, E. Villebrun and P. Hoeher, Proceedings of the IEEE International Conference on Communications, (1995) June 18-22; Seattle, USA
- [7] S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, TDA Progress Report, 42-127, 1 (1996).
- [8] O. Y. Takeshita, IEEE Trans. Inf. Theory, 52, 1249 (2006).