

High speed data acquisition and processing system for precipitation detection Based on linear CCD

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Abstract –In order to realize automatic observation of Precipitation, Optical precipitation auto-measurement system is designed based on linear image sensor. Considering the mass acquisition data which are inconvenient for transmission and processing under continuous operation, real-time binarization and encoding processing of linear image data are carried out by Field Programmable Gate Array (FPGA). Original data or encoding data can be transmitted based on TCP/IP protocols and Ethernet. Dual-ports RAM and internal FIFO are designed for data buffer unit and data compare unit in this system, so it can meet the demand for high speed data collecting, transfer and processing. The structure of the system is simple, low cost and has wide application prospect.

Keywords –Precipitation; Photoelectronic Measurement ; Image of raindrop; Linear CCD; FPGA

I. INTRODUCTION

Knowledge on details of hydrometeors is of vital importance in meteorology, in cloud physics, in the fields of telecommunications, explicitly to mention wave propagation and in remote sensing^[1]. Compared to many other instruments for measuring precipitation, such as the Scattering Spectrometer instruments^[2,1], lightning extinction instruments^[3,4], instruments based on optical image method have more advantages. Based on imaging technique, precipitation particle size and velocity can be measured simultaneously, as well as precipitation particle shape and oscillations can be examined^[5].

As size and speed of precipitation particles have wide range of different scales, in order to ensure the particles through the sample zone can obtain a certain number of scans, the line array sensor sampling rate should be more than 25000fps, the amount of real-time image acquisition is in proportion to linear scanning speed, so high-speed real-time mass data acquisition with reliable transmission is one of the key difficulties^[6].

In this paper, a line array precipitation measurement system hardware platform was established with FPGA (Field Programmable Gate Array) as the control center, and data acquisition and processing are also based on FPGA. Aiming at features of high linear scanning speed and large volume

real-time data collection, linear image data binarization and data encoding are carried out in FPGA, therefore high-speed mass storage and data in real time treatment can be realized. Logic resources and storage resources in FPGA are made full use of, real-time linear data comparing with threshold in dual-port RAM can generate corresponding binary data stream, then binary data stream are encoded for the purpose of further reducing the amount of data transmission and easing handling pressure of PC, so requirements of long-term continuous observation data storage and processing can be meet.

This paper will be structured as follows; In Section II we will introduce the system structure and its operating principle Section III we will describe data cache and data binarization in FPGA; In section IV, we will show a primary experimental result. Finally, Section V contains conclusions.

II. MEASURING DEVICES AND METHODS

The principles of the Optical precipitation measurement system are illustrated in Fig.1. The system is consists of three main units: the sensor unit, which consists of collimator unit and optical imaging unit; the collection unit, which realized the data collection, data processing and data transmission; the data terminal processor, which stores the data and give a graphic display.

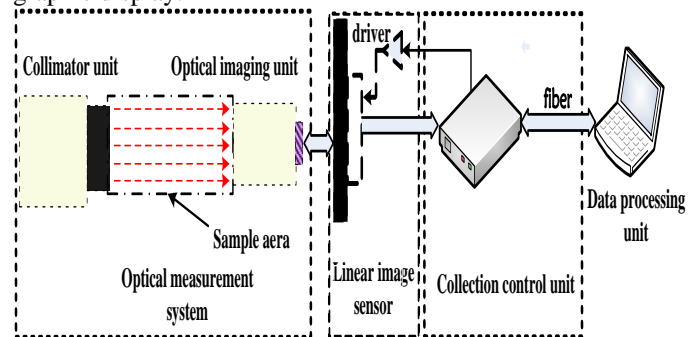


Fig.1 Block diagram of linear precipitation measuring system

The laser source (449nm, 30mW) produces a parallel light-beam between to the receiver spaced 15cm apart. The linear CCD with a lens is situated on the receiver in order to measure the optical intensity by transforming it into electrical signal. When a precipitation particle falls through the light

beam, the receiving signal is reduced. The size of the particle is determined from the maximum width across the array and particle velocity is determined by dividing the size of the particle by the amount of time it takes to cross the array. This is illustrated in the diagram in Fig.2 and Fig.3.

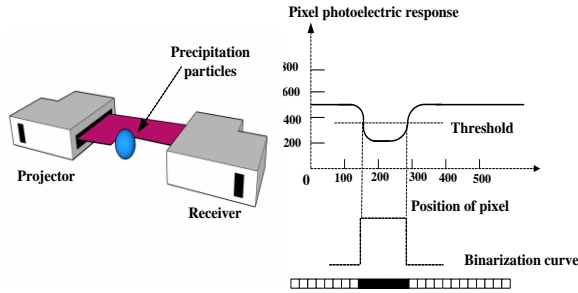


Fig.2 Diagram of particle imaging

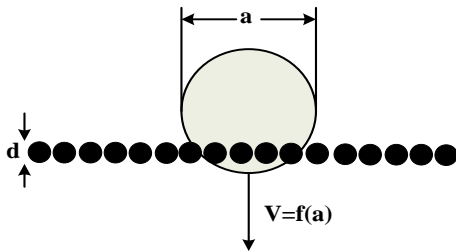


Fig.3 The particle size and fall velocity determined from the shadow

III. IMAGE DATA COLLECTION AND ENCODING IN FPGA

A. DATA CACHE MODULE AND LOGIC CONTROL

The timing for the CCD array is controlled directly from a Xilinx Spartan XC3S400, which is the core of the system. And high speed data collection and buffering, image data binarization and encoding, transmission interface protocol are designed and implemented in FPGA too. The Ethernet interface controller was designed with DM9000A.

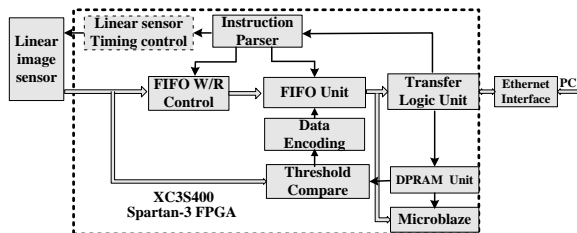


Fig.4. The diagram of functional module in FPGA

As illustrated in the diagram in Fig.4, the following functions are realized in FPGA: linear sensor timing control, FIFO W/R control, instruction parser, transfer logic unit, threshold compare and data encoding. Besides, storage resources in FPGA are used for FIFO and dual-port

RAM. The IP CORE offered by XILINX Corporation are tested carefully and occupies small resource. As for the FIFO IP, the FIFO IP CORE in FPGA was used for data transmitting among asynchronous clocks. There is no need for designing handshaking signals, FIFO read and write control signal can be designed according to corresponding state signal.

B. IMAGE BINARIZATION AND DATA ENCODING

According to Fig.2, the threshold is the key factor which can affect the horizontal projection size of the precipitation particle at the corresponding time. As for the binarization procedure, there are two ways, namely the special hardware circuit and software data processing [7]. Considering the characteristics of the high scanning speed of line array and large quantity of linear image data, linear image binarization and data encoding in FPGA chip is proposed.

With the logic resources and storage resources in FPGA, dual-port RAM IP core is used for the linear data binarization process. The binarization and data encoding procedure are as follows.

The Dual-port RAM is used to store the threshold, one port is used for the control terminal for writing the pre-set threshold, the other port can be read by the threshold comparison module. Take a fixed threshold set for example, when the pixel intensity corresponding value is lower than the threshold set in advance, the pixel is occluded completely, is set to 1. When all the pixels in a frame data are compared with the threshold, we can get the binarization curve which are composed 0 and 1.

As the binarization process is completed, we get the binarization curve and start the curve encoding process.

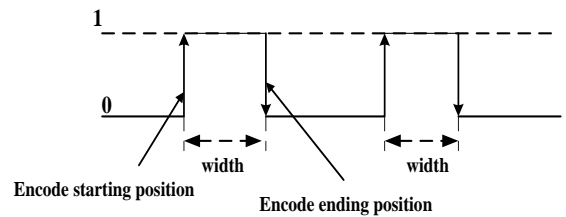


Fig.5. The diagram of encoding for the binarization curve

As illustrated in the diagram in Fig.5, when the rising edge of the binarization curve is detected, we start the counter for the width computing, which is corresponding to the number of occluded pixels of the precipitation particle. As the falling edge of the binarization curve is detected, we stop the counter and the counter is the number of the pixels shadowed by the precipitation particle. So the binarization curve can be expressed by the start position counter number and the ending position counter number. So the binary data stream is encoded for the purpose of further reducing the amount of data transmission and easing handling pressure of PC.

IV. EXPERIMENTAL RESULTS

Preliminary experimental verification is provided below.

The experimental verification setting are shown in Fig. 6, the main function of device comprises a collimator, an optical imaging lens, linear array sensor and data acquisition board and adjustable voltage source. The light source adopts a collimated laser light source with wavelength 495nm and power 30mW. Sampling rate of linear CCD image is 20000 frame /s.



Fig. 6 The experimental setup

The light source adopts a collimated laser light source with wavelength 495nm and power 30mW. Sampling rate of linear CCD image is 20000 frames /s. Light intensity of the parallel light source can be changed by adjusting the voltage source.

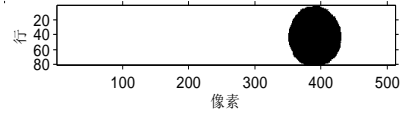
A STANDARD SPHERICAL PARTICLE IMAGING TEST

As illustrated in Fig.7 (a), the diameter of optical glass ball is 5mm and the refractive index is 1.5 which is close to the refractive index raindrops.

The glass ball down from the light beam 50cm above, when the glass ball falls through the light beam, the receiving signal is reduced; binarization curve of every frame according to the pre-settled threshold can be obtained. Then with all valid binarization curves, binarization image of the glass ball can be obtained, as shown in Fig.7 (b). As if the recorded image maybe elongated if the sample rate is too fast, the image shown in Fig.7 (b) has been adjusted [6].



(a)



(b)

Fig.7 Standard spherical particle imaging test

B. WATER SPRAY IMAGING TEST

As the glass ball is solid, we designed experiment for verification of the liquid particles. As illustrated in Fig.8 (a), a sprayer was about 10cm above the light beam, liquid particles of different

size can be generated. The original binarization image is shown in Fig.8(b).



(a)



(b)

Fig.8 Water spray imaging test

According to Fig.8 (b), we can see that the image is slightly elongated due to the sample rate is too fast. When the particles enter the sampling area and leave the sampling area, attenuation of the light intensity may be higher than the pre-settled threshold, so the upper and lower of the image are missing.

V. CONCLUSION

In order to realize untouchable measurement of precipitation particles, an optical precipitation measurement

system based on linear CCD image sensor was designed. Features of rich resources, flexible interface and parallel computing of FPGA were made best use in this system, combined with an Ethernet interface controller DM9000A, a stable and reliable high-speed data collection system has been realized. High-speed data acquisition and data encoding in real-time based on Xilinx's FPGA XC3S400 is designed in the system. It can obtain original data of linear CCD image data as well as the binarization data. With the threshold pestered, data comparing and encoding can be realized in real-time. Original data or encoding data can be transmitted according to requirement. Dual-ports RAM and FIFO are designed in this system for data buffer unit and data compare unit, so it can meet the demand for high speed data collecting, transfer and processing. The structure of the system is simple, low cost and has wide application prospect.

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