An Improvement Method for Efficiency and Stability of Circuit Fault Simulation

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Abstract

The paper briefly introduces the method and principle of circuit fault simulation and circuit functional reliability simulation, describes the problems of such method in engineering application, analyzes the reasons for such problems in detail, and advances relevant improvement method and measures pertinent to different reasons. Finally comparative simulation analysis is made for a typical case by the improvement method to validate it and verify the engineering application value of the technique.

Keywords: circuit; fault simulation; functional reliability simulation; reliability

1. Introduction

In the recent scores of years, electronic technologies have developed very rapidly. Currently electronic system design is developing toward quick speed, large capacity, small volume and light weight. OrCAD/Pspice, Mentor Graphics, VHDL, Protel, Electronics Workbench and other simulation software emerging thereupon lay firm foundation for the realization and popularization of Electronic Design Automation (EDA). Electronic system design and development by such software can sharply shorten system design cycle and improve product competitiveness.

Circuit fault simulation [1-3] is a valid method developed in such environment and for integrated design and analysis of system performance and reliability by EDA simulation and fault injection. Based on EDA simulation, it establishes circuit fault simulation model for the influence of circuit injection element failure, parameter drift, temperature change and other factors, and then gets the response output result after fault injection to circuit by simulation, further, provides data support for system performance and reliability analysis. The technique designs performance, meanwhile, helps the designers discover system design defects and potential faults as early as possible by fault injection method based on EDA software, and effectively validates system fault tolerance. Meanwhile, lots of fault response data acquired by fault simulation can be used for product test analysis, fault dictionary generation, etc.

The technique above has been mature in theoretical research, successfully applied to typical cases and recognized by circuit designers. However, in engineering practice, some problems, e.g. poor stability of simulation calculation, heavy load of simulation calculation and long simulation time, may occur when it's applied to a complex circuit. In respect of this, the paper mainly analyzes the reasons for such problems, and advances an improvement method accordingly. Additionally feasibility and effectiveness of the method are validated through the application to 1 practical circuit via circuit functional reliability simulation platform to verify the practical value of circuit fault simulation technique.

2. Reasons for problems

Simulation error, simulation halt, long simulation time and other problems may occur during circuit fault simulation and reliability analysis by circuit functional reliability simulation technique mainly for the 2 kinds of reasons as follows:

(1) Deficiency of circuit and simulation software

For circuit performance and reliability simulation, EDA simulation software first reads information of circuit diagram, and then converts circuit network structure into relevant system of equations by Kirchhoff's voltage law and current law, later resolves the system of equations by mathematical methods (e.g. numerical integration method, main element elimination method), and solves matrix equation. Normally it takes some time to get circuit simulation result, the larger and more complex a circuit is, the longer its simulation time will be. Especially normal element parameter value may be set as limit value during fault injection to circuit, as a result, numerical calculation generates stiff equation greatly prolonging simulation time. Just because of special requirement of numerical calculation for stability, every kind of circuit simulation software has own restriction principle, e.g. a circuit shall be free of directly closed loop of power source and earth, and breach of such rules usually cause simulation failure or wrong simulation result.

(2) Deficiency of analysis method and control algorithm

As stated in the Introduction, reliability analysis tools of circuit functional reliability simulation platform include multiple analysis methods, and every kind of analysis method needs much fault injection, i.e. every kind of failure mode is injected, further, statistical analysis is made by circulation and sampling. For a medium circuit with about 200 elements, its total number of failure modes may be up to 3,000 pieces or above, as causes the acute expansion of simulation time.

3. Study on improvement method

3.1. Principles for improvement method

In order to enhance the applicability of circuit fault simulation method to engineering, suitable improvement method should be adopted. Such improvement mainly follows the principles as follows:

(1) Improving circuit simulation mechanism

Pertinent to the objective reason involving EDA tool and system scale, circuit simulation mechanism is improved so that it can fundamentally shorten simulation time and improve simulation stability on the principles as follows:

- Reduce the time of per simulation to shorten total simulation time;
- Raise simulation speed to decrease times of simulation overflow;
- Enhance the stability of per simulation.

(2) Selecting efficient control algorithm

Pertinent to the subjective reason involving simulation time expansion by excessive simulation times caused by control algorithm, the algorithm is optimized to shorten total simulation time on the 2 principles as follows:

- Decrease simulation times;
- Raise sampling efficiency.

3.2. Improvement measures

On the improvement principles above, essence of circuit parameter calculation by EDA tool and characteristics of reliability analysis algorithm are seriously analyzed, and the following 5 improvement measures are discovered to enhance system simulation stability, raise system simulation efficiency and reduce simulation time.

(1) Layered simulation is adopted, i.e. a complex circuit is broken down into several subcircuits for separate simulation to reduce time of per simulation and shorten total simulation time.

In essence, circuit simulation by EDA circuit simulation software is to convert information of circuit structure into differential equation set of circuit, and resolve it by numerical method. The more complex a circuit is, the more equations needing iterative solution will be, and the longer the resolving time will be. Resolving time and number of circuit nodes are in extremely high linear growth relation. Hence a complex circuit may be broken down for separate simulation in certain case to shorten simulation time. Principles for circuit breakdown are as follows:

- No signal feedbacks exist among subcircuits;
- Signal feedbacks exist among subcircuits, but feedback signal doesn't affect the next level of input signal or form closed loop signal feedback.

For example, the complex circuit shown in Fig. 1 is broken down into the 2 subcircuits Part1 and Part2 shown in Fig. 2, then V(B1) is required to affect neither V(A1) nor V(A2). Later separate simulation is conducted for them, and V(OUT) is tested.

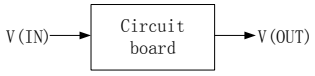

Fig. 1: Schematic Diagram of Whole Complex Circuit Board.

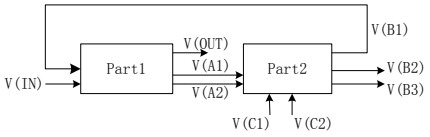

Fig. 2: Schematic Diagram of Complex Circuit Breakdown

(2) Reasonable simulation setting is selected to raise simulation speed and decrease times of simulation overflow.

In EDA software, there are many parameters [4] concerning calculation accuracy, iteration times, time step and others and also closely correlated with simulation run time and simulation accuracy. For example, there are calculation accuracy parameter RELTOL, voltage accuracy parameter and others in OrCAD/PSpice software. The smaller the parameter values above are, the higher the accuracy requirements will be, and the larger the iteration times of calculation will be, so the longer the simulation run time will be. Thereof, RELTOL default value is 0.001 and higher than required accuracy, if it's changed into 0.01, the calculation speed can be raised by 1.5 times. Normally its value is set as 0.01 to meet simulation requirement in the case that accuracy isn't highly emphasized. Node iteration times ITL4 is also a key parameter influencing simulation time, the larger the iteration times is, the longer the simulation time will be, normally it's set as 20 or so and within 50, otherwise simulation time will be wasted, moreover, the acquisition probability of resolving result won't be greatly increased. Meanwhile, on the premise that all simulating settings are fixed, if the resolving result of equation is still unacquirable when both specified accuracy requirement and iteration times reach boundary conditions, simulation overflow will occur and cause the simulation to fail.

Therefore, for simulation setting, circuit's simulation time, simulation accuracy and simulation stability requirements shall be considered referring to the principles as follows: On the premise of meeting design and analysis requirements,

- Parameter value of relative accuracy shall be as large as possible;
- Iteration times shall not be too small;
- Simulation time shall be set as short as possible;
- Max. time step shall be maximum as possible.

(3) Suitable failure mode shall be selected to meet software restriction principle, reduce probability of simulation overflow and enhance simulation stability.

In respect of the restriction principle for circuit simulation software, circuit fault simulation model formed during fault simulation shall meet software requirements, free of zero resistance loop, hanging node of analog device, etc. When failure mode is selected for injection, attention shall be paid to avoiding short circuit of power source and earth and other similar faults prone to causing simulation halt.

(4) Event drive replaces for time drive to decrease simulation times.

Reliability is a function related to time, so it's necessary to sample time on time axis during reliability analysis of electronic system by fault simulation, and a clock shall be set. With the run of simulation, the analog clock keeps stepping. Normally clock stepping adopts fixed time increment method, i.e. the clock always steps by fixed time unit during the run of simulation. In every time interval, the system shall conduct 1 time of query and judgment. During reliability analysis, total simulation time is very long, moreover, in order to avoid the simultaneous occurrence of different events, fixed time increment shall be as small as possible, as causes large times of system query. In order to decrease simulation times, fixed time increment is replaced by next event increment for clock management. Namely time stepping point is only defined at the occurrence time of event, and analog clock is always advanced to the point of time of the nearest next event, so time advance only relies on occurrence of event, as sharply decreases system query times and shortens simulation run time. Fig. 3 shows relation between actual event and 2 kinds of time process management during simulation.

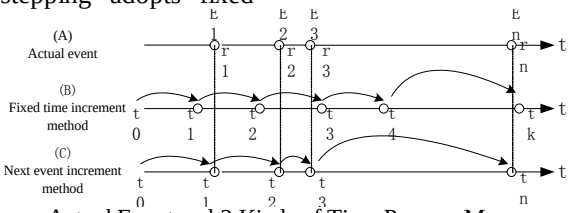

Fig. 3: Relation between Actual Event and 2 Kinds of Time Process Management

(5) For random variable sampling, stratified sampling replaces for simple sampling to raise sampling efficiency.

Algorithm of circuit functional reliability simulation analysis hides some problems of random variable sampling. For example, to identify the failure mode of element causing a circuit fault, failed element may be first sampled according to failure rate, and then failure mode of such element may be sampled. This way is much more efficient than simple sampling method.

4. Application effect of improvement method

Take control subassembly circuit as an example, its signal transmission is shown in Fig. 4. Its reliability simulation is validated by the improvement method advanced in the paper. Input signals of control subassembly are command signal and data signal transmitted by flight control computer of stable loop, decoded in signal reception and command conversion circuit (PART1), and then transmitted to channel and controlpiston voltage forming circuit (PART2) for D/A conversion and amplification, finally outputted to in-

terface subassembly of stable loop. Thereof, only when control subassembly conducts self-check, PART2 transmits status signal to PART1 for self-check, and self-check result is formed in PART1 and directly outputted.

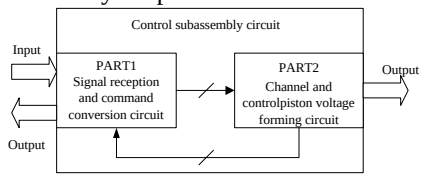

Fig. 4: Signal Transmission in Control Subassembly Circuit

Layered simulation method is used. Overall simulation model of control subassembly circuit and split PART1 and PART2 simulation models are established respectively to evaluate their self-check function and validate simulation. Layered fault simulation scheme:

(1) Conduct fault simulation for PART1, take the output as signal input in PART2, next conduct normal simulation for PART2, take the new output as signal input in PART1, finally conduct fault simulation for PART1.

(2) Conduct fault simulation for PART2, take the output as signal input in PART1, and then conduct normal simulation for PART1.

Through preliminary debugging and test, parameter values of RELTOL and ITL4 in circuit simulation setting are corrected to decrease times of simulation overflow and eliminate some fault modes causing simulation halt (e.g. short circuit with power source). Finally 600 typical failure modes in control subassembly circuit are injected for overall and layered fault simulations respectively. Such simulations are normal, and get the same result. As to simulation run time, overall simulation of control subassembly circuit takes 15 to 17 min, separate simulation of PART1 takes about 3min, and that of PART2 takes about 40s to 1min, hence simulation time of layered simulation method shortens overall circuit simulation time by nearly 75%.

Thereupon reliability analysis is made by time drive and event drive as well as simple sampling method and stratified sampling method respectively, and then circuit reliability curves are drawn. According to simulation results, their curves are consistent, the former takes 10min, and the latter takes 5min plus 40s, hence optimized simulation algorithm can nearly double simulation efficiency.

5. Conclusion

Circuit fault simulation is core technique for circuit functional reliability simulation. Its applicability directly influences the degree of engineering application of circuit functional reliability simulation technique. The paper analyzes the problems of circuit fault simulation method in practice, and studies relevant improvement method and advances improvement measures. At last, the improvement method is applied to an engineering case, and the simulation test result shows the improvement measures have an obvious effect, as paves the way for further application of circuit functional reliability simulation technique.

6. References

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