National College Students Innovation Project: The Design of a Programmable Filter Using FPGA

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Abstract. In this paper, the method of designing a programmable filter using FPGA was suggested. Due to its high efficiency and performance, FPGA chip was used control MF10 chip. The results showed high accuracies in filtering. The amplification of input signals, the filtering types and the -3dB frequency of filter were adjusted and controlled by the keys. The project accomplished the objective to improve the abilities of college students to analyze and solve problems independently.

Introduction

With the development of information technology, filtering is now playing important roles in the fields of data collecting, signal processing, communication system and engineering test. For example, in an engineering test, the test signals often come with noises. Besides enhancing the strength of desired signals, suppressing disruptions and increasing the Signal to Noise Ratio (SNR), employing filtering on test signals is also an efficient way to increase the SNR[1,2]. This is due to the differences in frequency bands between desired signals and the noises. Without distorting the desired signals, properly using these differences to suppress the noise signals will increase the SNR notably[3,4]. Up until now, few studies regarding programmable filters have been done. Different resistor–capacitor circuits (RC circuits) were used to build earlier programmable filters, which had the drawbacks of high circuit complexity, low accuracy and low stability[5].

System Design

Fig.1 shows the system design block diagram. This system was consisted of single chip, programmable filter chip, clock generator, programmable amplifier.

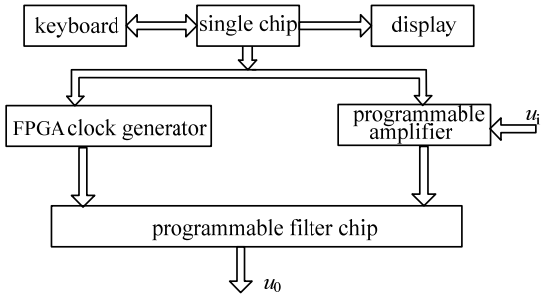

Fig.1 The system block diagram

Amplifier Design. The signals sampled are usually weak and hence can be easily disrupted. Therefore, it is necessary to amplify these weak signals. In this study, normal operational amplifier LF353 was used to set up a two-stage amplifier circuit. The amplification range was 0-60 dB with a step of 10 dB. The amplification factor was controlled by a single chip. The error was smaller than 5%. The programmable amplifier circuit was shown in Fig.2.

When the first stage amplifier was connected to A_1, the voltage gains A_u= 3.2 (i.e. 10 dB), where error was 1.03%; when connected to A_2, the voltage gains were 20 dB; when connected to A_3, the voltage gains were 30 dB. In sum, connecting the first stage amplifier to different ports (A_0-A_3) led

to maximum voltage gains of 30 dB with a step of 10 dB. Therefore, a two-stage amplifier will achieve maximum voltages of 60 dB. The error due to the differences in resistance values is approximately 1%. The maximum error of a one-stage amplifier is 3%; and that of a two-stage amplifier is 4.2%, which meets the requirements.

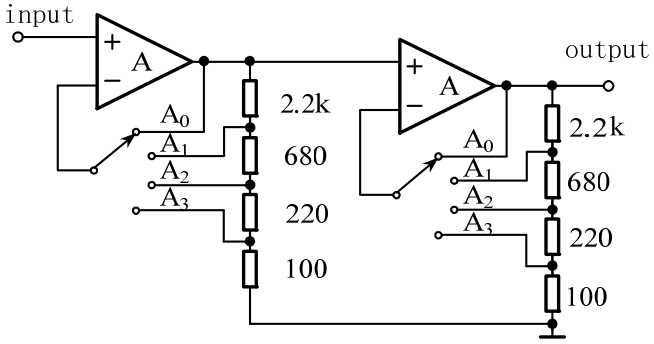

Fig.2 The circuit of programmable amplifier

Filter Design Based on MF10. Switched capacitor filter chip MF10 can be used to achieve various kinds of filtering while connected to small amount of resistive elements. In addition, MF10 is able to filter in a wide frequency band range, which is practically desirable. Therefore, MF10 was selected as the filtering chip in this study. The diagram of the filtering system is shown in Fig.3.

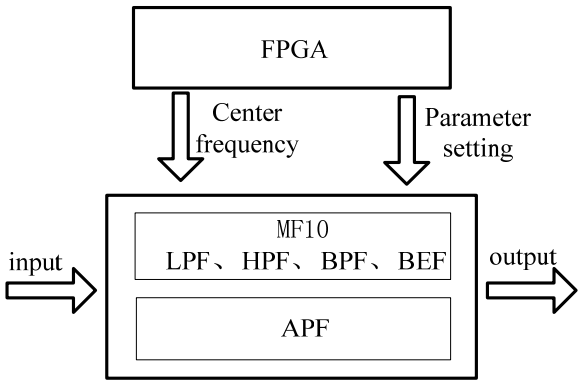

Fig.3 Diagram of the filtering system

MF10, as an MOS switched capacitor filter chip, consists of two independent filter modules. It can form a first-order or second-order filter; and if cascaded, a fourth-order filter. Each circuit has multiple filtering types, which can be controlled by adjusting the peripheral circuit of the chip. The chip needs an external clock to control the central frequency of the band-pass or band-stop filter. The cutoff frequency of the filter will be precise as long as the external clock has high precision.

Fig.4 shows the detailed MF10 circuit(after debugging) used in this study. It has low-pass, band-pass, band-stop and high-pass four filtering types.

Clock Generator Based on FPGA. In order to obtain filterings of high precisions from MF10, it is necessary to provide a high-precision external control frequency whose duty ratio is 50%. As long as the precision of the control frequency is adequately high, the precision of the-3dB frequency of MF10 will reach a corresponding high level. FPGA is a parallel running logic device with high operating frequencies, fast execution speed and highly stable performance. Therefore, it is a good fit for providing MF10 with external control frequencies.

FPGA chip EP1C3T144C8 was used to provide with external control frequency to MF10. This chip has built-in phase-locked loop that serves as the frequency multiplier of the input clock. The working principle of FPGA clock generator is shown in Fig.5.

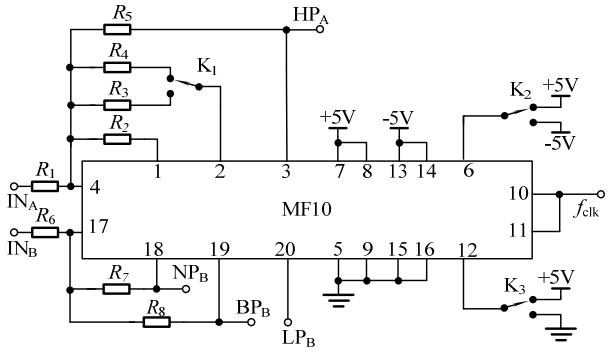

Fig.4 The filter based on MF10

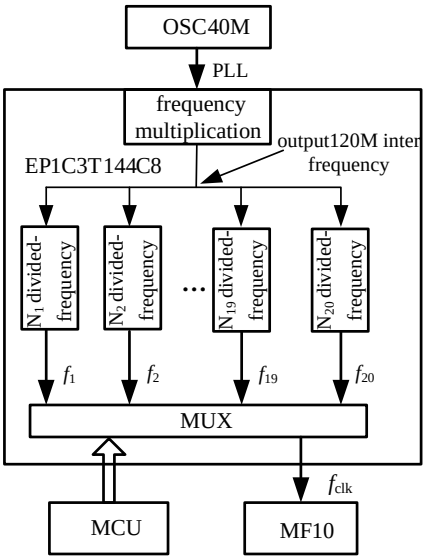

Fig.5 The block diagram of FPGA clock generator

As shown in Fig.5, the external crystal of FPGA was 40MHz. This clock frequency was first inputted into the built-in phase-locked loop of FPGA. Then the phase-locked loop tripled this frequency and outputted an internal working clock of 120MHz. Due to the objective of this project of achieving filtering with 20 different -3dB frequencies (1 kHz– 20 kHz), FPGA was used to provide MF10 with 20 different external control clocks. This was achieved by applying 20 different frequency divisions on the 120MHz internal working frequency outputted by the phase-locked loop. Then these 20 frequencies were inputted into the multiplexer inside FPGA. With which frequency MF10 was to be provided was determined by the command from the single chip. In this way, the -3dB frequencies changing from 1kHz to 20kHz by a step of 1 kHz was achieved.

MF10 works differently when employed to conduct different types of filters, which requires different design of peripheral circuits. This leads to different R_2, R_3, R_4 resistances and Q values. Even if R_2, R_3 and R_4 have the same resistance, different f_c equations are used when MF10 conducts different types of filters. Therefore, the external control frequencies cannot be the same. For example, a high-pass 20 kHz filtering requires an external control clock frequency of 1 MHz while a low-pass 20 kHz filtering may only require an external control clock frequency of 980 kHz. Therefore, the 20 control frequencies used in the high-pass filtering cannot be used to control the low-pass filtering. So FPGA should provide different groups of 20 different frequencies for different types of filters. Only in this way can MF10 achieve high precisions when dealing with different types of filters.

Design of Control and Display Circuits. Keys are needed to control the preamplifier, the filtering types and the -3dB frequencies of the filter. In addition, the display function is necessary in order to allow users be aware of in which operation condition the system currently is. This system employed 6 keys to control the preamplifiers, the filtering types and the -3dB frequencies of the filter. Then the current operation condition was displayed on a LCD display. This was accomplished using the single chip. The diagram of this part of the system is shown in Fig.6.

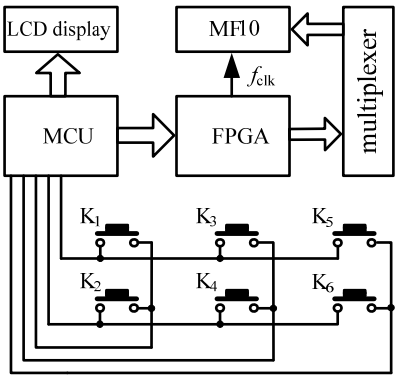

Fig.6 The control and display diagram

Fig.7 The prototype of the programmable filter

In Fig.6, key K_1 or K_2 was used to increase or decrease the amplification, respectively; K_3 and K_4 were designed to control the types of filters; K_5 and K_6 were used to change the -3dB frequencies.

Conclusions

After debugging, the programmable filter design was accomplished. The prototype is shown in Fig.7.

This study was beneficial for college students in terms of developing practical skills and innovation spirits.

References

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