A Backscatter Link Frequency Algorithm with High Stability for Passive UHF RFID Tags

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Keywords: UHF RFID tag, Backscatter link frequency (BLF), National Protocols, high stability.

Abstract. This paper introduces a backscatter link frequency (BLF) algorithm featuring high stability for passive UHF RFID tags, which is fully compatible with Information technology -Radio frequency identification- Air interface protocol at 800/900 MHz(GB/T 29768-2013) called National Protocols. Not only are constraint conditions of backscatter link communication taken into account, but also influences of system clock error, counting errors and dividing errors are considered. What's more, the certain range of clock frequency is provided by the proposed algorithm and the BLF keeps stable. Simulation results show that the produced backscatter link frequency errors is less than 20% with the system clock from 1.2MHz to 4MHz.

Introduction

With the development of Internet of Things, Radio frequency identification (RFID) technology becomes pervasive in a wide range of domains including logistics and supply chain management, building management and animal detection areas. National Protocols is the first specification of air interface communication at 860-960MHz in respect to RFID in china, which makes difference to the development of RFID.

Since the BLF signal takes the major responsibility to make the backscatter link communication from tag to reader successfully, it's of great important to design a baseband with BLFs that has ability of high stability.

Usually, the BLFs are generated by dividing the system clock [1]. The National Protocols require the frequency error of the backscatter link within ±20% [2]. It is difficult for a free-running oscillator to achieve this accuracy since the frequency deviation of a typical oscillator can be as much as ±20%, which alters with variations of process, voltage and temperature (PVT) [3], [4]. One of the critical challenges is a system clock with the stringent accuracy needed for dividing. The reported solutions to achieve accurate system clock is making improvements by analog method or digital method, such as adding clock calibration circuit [5], temperature compensation [6] and preamble training [7]. However, these methods either consume more power or occupy more resources.

In this paper, a baseband BLF algorithm is put forward basing on a detailed analysis of the specified BLF, which has merits of lower requirement of clock accuracy and resources, and high stability under frequency deviation.

The rest of the paper is organized as follows: Section 2 presents the National Protocols fundamental; Section 3 proposes the backscatter link frequency algorithm and error analysis; Section 4 gives the simulation results and comparisons. At last, Section 5 is the conclusion of the paper.

National Protocols Fundamental

The National Protocols specifies the air interface between reader and tag. All commands sent by the readers are followed by a preamble depicted in Fig. 1, which consists a fixed-length start delimiter, calibration symbol I and calibration symbol II, Where T_C will be 6.25μs or 12.5μs.

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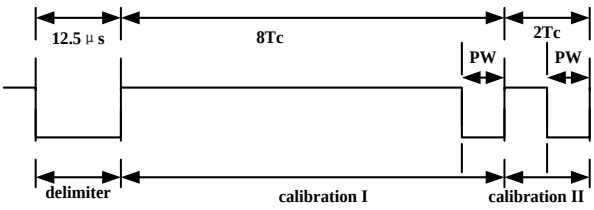

Fig. 1 Preamble Send by Reader

The backscatter link communication uses a fixed BLF for the duration of an inventory round. The tag's BLF is decided by backscatter link frequency coefficient (*K*) of the Query command. Equation (1) specifies the relationship between BLF_{pri} and *K*, as follows:

$$BLF_{pri} = {1}/{T_{pri}} = 320KHz \times K \tag{1}$$

Where BLF_{pri}, T_{pri} is the specified backscatter link frequency and clock. The values of *K* are shown in Table 1, which is set in the Query command. The tag computes BLF and makes it closing to BLF_{pri}. For tags certified to the protocol, they shall support all the BLFs and FE specified in Table 1.

Table 1 Backscatter Link Frequencies and Tolerances

Backscatter Link Frequency coefficient (*K*)	BLF(kHz)	Frequency Error (*FE*)
1/5	64	-20%～20%
3/7	137.14	-20%～20%
6/11	174.55	-20%～20%
1	320	-20%～20%
2/5	128	-20%～20%
6/7	274.29	-20%～20%
12/11	349.09	-20%～20%
2	640	-20%～20%

Proposed Backscatter Link Frequency Algorithm

The Analysis of Backscatter Link Frequency Algorithm. According to the National Protocols, the frequency errors of the backscatter link at all set frequencies is within ±20%, which means the system clock variation should be less than ±20%.

To implement all backscatter link frequencies, a simplified architecture is depicted in Figure 2, which is made up of three blocks: an RC oscillator, an algorithm module and a divider, while architecture of [8] is shown in Fig. 3, there are four blocks. Since the Proposed Algorithm has high stability, improvements of system clock are useless, and less resource is required.

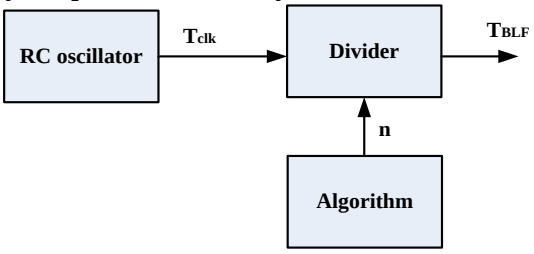

Fig.2 Architecture of this work

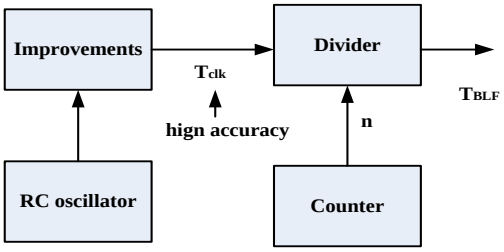

Fig.3 Architecture of [8]

The BLF is generated by the clock signal from the oscillator expressed by Eq. (2), where T_{clk}, T_{BLF} are system clock and backscatter link clock, respectively, and n is divide ratio.

$$T_{BLF} = n \times T_{clk} \tag{2}$$

Comparing with Eq. (1), divide radio is got by combining *K* with calibration symbol II which is treated as a reference for the system clock. Since T_C has two values of 6.25μs and 12.5μs, detail analysis of the divide ratio with T_C =6.25μs and T_C =12.5μs are presented respectively.

- when T_C =6.25μs

Step 1: Making some adjustments in the Eq. (1) with T_C, and rewriting the Eq. (1) in the way of T_{BLF}.

$$T_{BLF} = \frac{1}{320KHz \times K} = \frac{1}{\frac{2}{T_C} \times K} \tag{3}$$

Step 2: A key step in the Algorithm is to make use of the length of calibration symbol II (N_{cal2}) to calibrate the clock (T_{clk}). Counting the number of rising clock edges during calibration symbol II period and the counts keep the digital value of calibration symbol II as N^{nom}. In this equation, the value of T_{clk} is $2T_C$.

$$N^{nom} = \frac{N_{cal2}}{T_{clk}} \tag{4}$$

Step 3: Combining with Eq. (4), and make some substitutions in Eq. (3), the backscatter link clock (T_{BLF}) can be expressed in Eq. (5), comparing Eq. (5) with Eq. (2), the divide ratio (n^{nom}) can be got.

$$T_{BLF} = \frac{N^{nom}}{4 \times K} \times T_{clk} \tag{5}$$

$$n^{nom} = \frac{N^{nom}}{4 \times K} \tag{6}$$

Step 4: As the National Protocols specified, tolerances on calibration symbol II specified in the units of T_C shall be ±1% [2]. When the tolerances are taken into consideration, $N_{\max}^{nom}$ and $N_{\min}^{nom}$ represent the maximum and minimum value of N^{nom}, respectively. The minimum and maximum of the divide ratio n are expressed as below:

$$n_{nim} = round(\frac{N_{\min}^{nom}}{4 \times K}) \tag{7}$$

$$n_{\max} = round(\frac{N_{\max}^{nom}}{4 \times K}) \tag{8}$$

Where $N_{\min}^{nom} = 0.99 \times N^{nom}$ and $N_{\max}^{nom} = 1.01 \times N^{nom}$.

- when T_C =12.5μs

As a result of a twice relation between the two values of T_C, it can be rewritten the Eq. (1) in the same way, the produced backscatter link clock (T_{BLF}) is shown as follows:

$$T_{BLF} = \frac{1}{\frac{4}{T_C} \times K} = \frac{N^{nom}}{8 \times k} \times T_{clk} \tag{9}$$

The normal, minimum and maximum of divide ratio can be respectively expressed as

$$n^{nom} = \frac{N^{nom}}{8 \times K} \tag{10}$$

$$n_{nim} = round(\frac{N_{\min}^{nom}}{8 \times K}) \tag{11}$$

$$n_{\max} = round(\frac{N_{\max}^{nom}}{4 \times K}) \tag{12}$$

Error Analysis.

(1) Error Introduced by System Clock

The system clock takes more responsibilities when the baseband circuit manages to calibrate the BLF. In the paper, a typical oscillator without any other improved circuit which is in the point of low-power design is used. As is known, the variation of the system clock is mainly caused by the variations of PVT, which can be as high as ±20%. Therefore, the backscatter link frequency errors are introduced inevitably under the influence of imprecise system clock.

(2) Counting Errors

A digital counter is usually implemented to measure N_{cal2} by counting the positive or negative edges. The symbols are asynchronous signal to the clock signal of the circuit, which can introduce counting errors [8]. Simply, supposing only the high level of the symbol is measured, and is counted at the rising edges of the clock signal, an example is shown in Fig. 4. The length of Symbol A is more than 3 clock periods, but it is counted as 3, thus it has a count error between the counts and the real length.

(3) Dividing Errors

The BLFs is produced by dividing the system clock. A frequency divider in the form of digital counter use a dividing ratio which is calculated by a round(x) function to count the system clock, thus the produced BLF may be different from the specified BLF demanded in the Eq. (1). As a result, intrinsic quantization errors are introduced, which is called dividing errors.

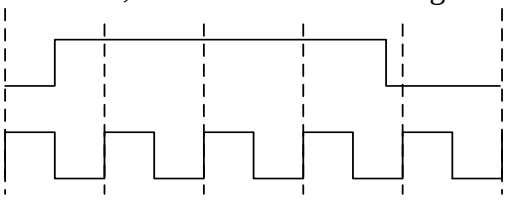

Fig. 4 Lengths of symbol measured by clock counts

The Frequency Error (*FE*) of Backscatter Link Frequency Algorithm. The FE of backscatter link is defined in Eq. (13), Where T_{BLF}^{nom} represents the specified backscatter link clock comparing to the produced backscatter link clock T_{BLF}.

$$\left|FE\right| = \left|T_{BLF}^{nom} - nT_{clk}\right| \Big/ T_{BLF} \tag{13}$$

According to the analysis of BLF errors, some adjustments are made in Eq. (13) with Eq. (7), Eq. (8), Eq. (11), Eq. (12), $FE1$ is the minimum of FE while $FE2$ is the maximum of FE.

$$\left|FE1\right| = \left|T_{BLF}^{nom} - n_{\min}T_{clk}\right| \Big/ T_{BLF} \tag{14}$$

$$\left|FE2\right| = \left|T_{BLF}^{nom} - n_{\max}T_{clk}\right| \Big/ T_{BLF} \tag{15}$$

As a matter of fact, it's necessary to make sure that the largest value of FE computed by Eq. (16) is in accordance with the specification of the National protocols, where $\left|FE_{\max}\right| \le 20\%$.

$$\left|FE_{\max}\right| = \max\left\{\left|FE1\right|, \left|FE2\right|\right\} \tag{16}$$

Simulation Results and Comparisons

The algorithm has been verified in the MATLAB and the BLF error curves are plotted. Comparing Eq. (6) with Eq. (12), it comes to a conclusion that the BLFs are not under the influence of T_C, so that the error curves with T_C =6.25μs are the same as T_C =12.5μs. As shown in Figure 5, the BLF errors curves for all different BLFs are respectively plotted， e.g. (a), when K is 1/5, the produced BLF is about 64 kHz, the curve shows that the FE is below 20%. The results prove that the algorithm has completely coherency with the National protocols in a system clock range from 1.2 MHz to 4 MHz.

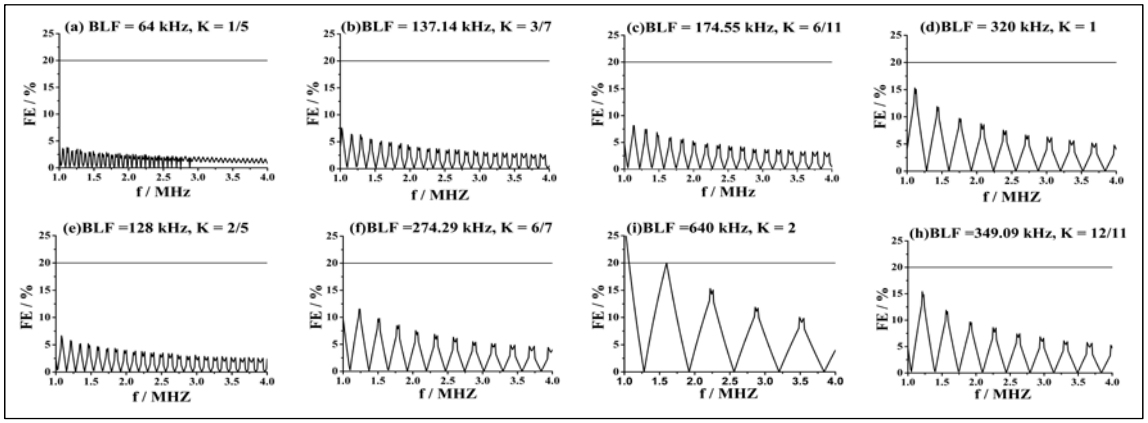

Fig.5 FEs for (a) K=1/5, (b) K=3/7, (c) K=6/12, (d) K=1, (e) K=2/5, (f) K=6/7, (h) K=12/11, (i) K=2

Summary

A high stability backscatter link frequency algorithm complying with the National protocols is presented, has lower demands for the system clock. Simulation Results show that the produced backscatter link frequency errors are less than 20% and the produced BLFs are stable when the system clock between 1.2 MHz and 4 MHz. Furthermore, the algorithm has advantages of lower requirement of clock accuracy, less required resources.

Table 2 Comparisons

References	Frequency(MHz)	Additional resources
[9]	1.92	yes
[10]	1.92	yes
This work	1.2-4	no

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